

1. Schematic Page Description :

ZHS/BTM-origins Schematic Ver :

- | | |
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| 03 -- Valley 1/9 (DDRA) | 23 -- TPM /LED |
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| 05 -- Valley 3/9 (Display) | 25 -- Audio Codec |
| 06 -- Valley 4/9 (SD/PCIE/SATA) | 26 -- USB3/Charger/Hole |
| 07 -- Valley 5/9 (SPI/GPIO/CLK) | 27 -- KB/TP/HW RST |
| 08 -- Valley 6/9 (USB/LPC/I2C) | 28 -- KBC |
| 09 -- Valley 7/9 (Power 1) | 29 -- Charger (BQ24715RGRR) |
| 10 -- Valley 8/9 (Power 2) | 30 -- SYSTEM 5V/3V (MPS670/671) |
| 11 -- Valley 9/9 (GND) | 31 -- Load Switch |
| 12 -- BTM XDP & APS | 32 -- DDR 1.35V(TPS51216) |
| 13 -- DDR3L MEMORY DOWNx16 CHA | 33 -- +1.05V/+1V(TPS54318) |
| 14 -- DDR3L MEMORY DOWNx16 CHB | 34 -- +VCC_CORE(ISL95833) |
| 15 -- Level Shifter (SOC_EC) | 35 -- LDO-1 (G9661) |
| 16 -- Level Shifter (SOC_DEV) | 36 -- LDO-2 (G9661) |
| 17 -- SDIO CardReader | 37 -- Thermal protect |
| 18 -- LCD/CCD/DMIC | 38 -- Power Sequence |
| 19 -- Google Debug | 39 -- SMBUS/I2C |
| 20 -- HDMI | 40 -- BTM PWR TREE |
| | 41 -- Change List |

I2C table

Function	Channel	Read	Write
Touch pad	I2C0	0x67	
Audio codec	I2C1	0x21	0x20
Light sensor	I2C4		

SMBus table

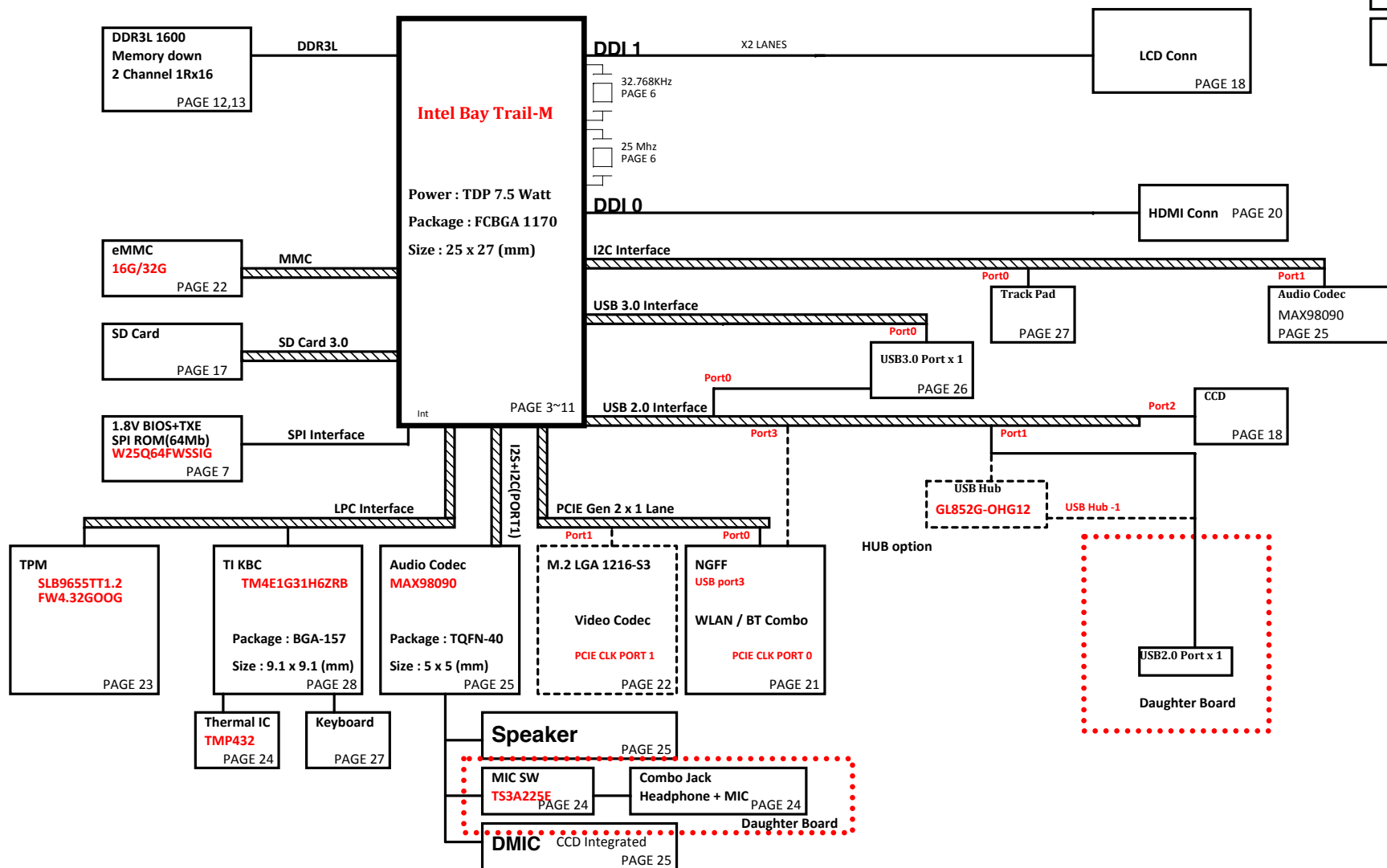
Function	Channel	Address
Battery	SMB0	
Thermal	SMB2	0x4C

Function	Channel
PP3300_DSW	0x42
PP5000	0x41
PP1350	0x49
PP1050_PCH	0x43
PP1000_PCH	0x47

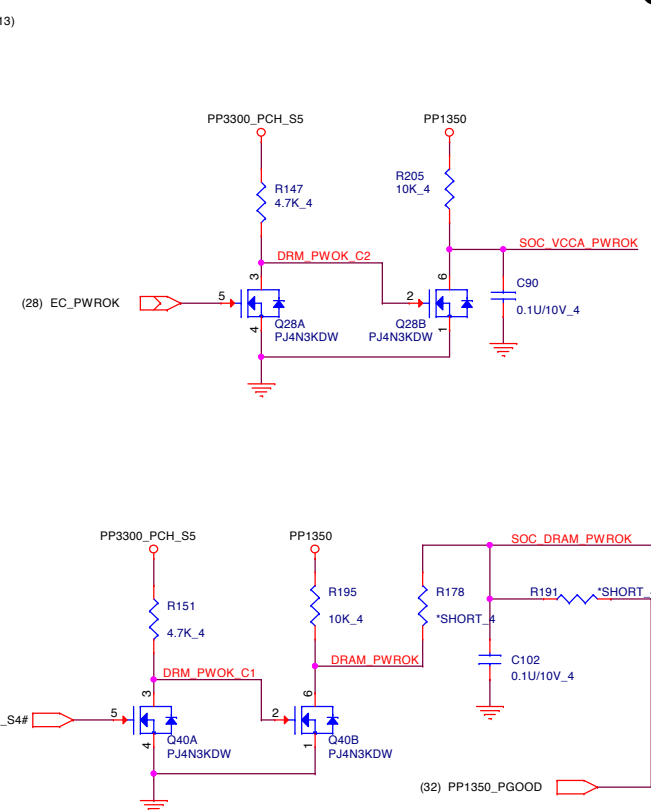
ZHR/BTM-Origins

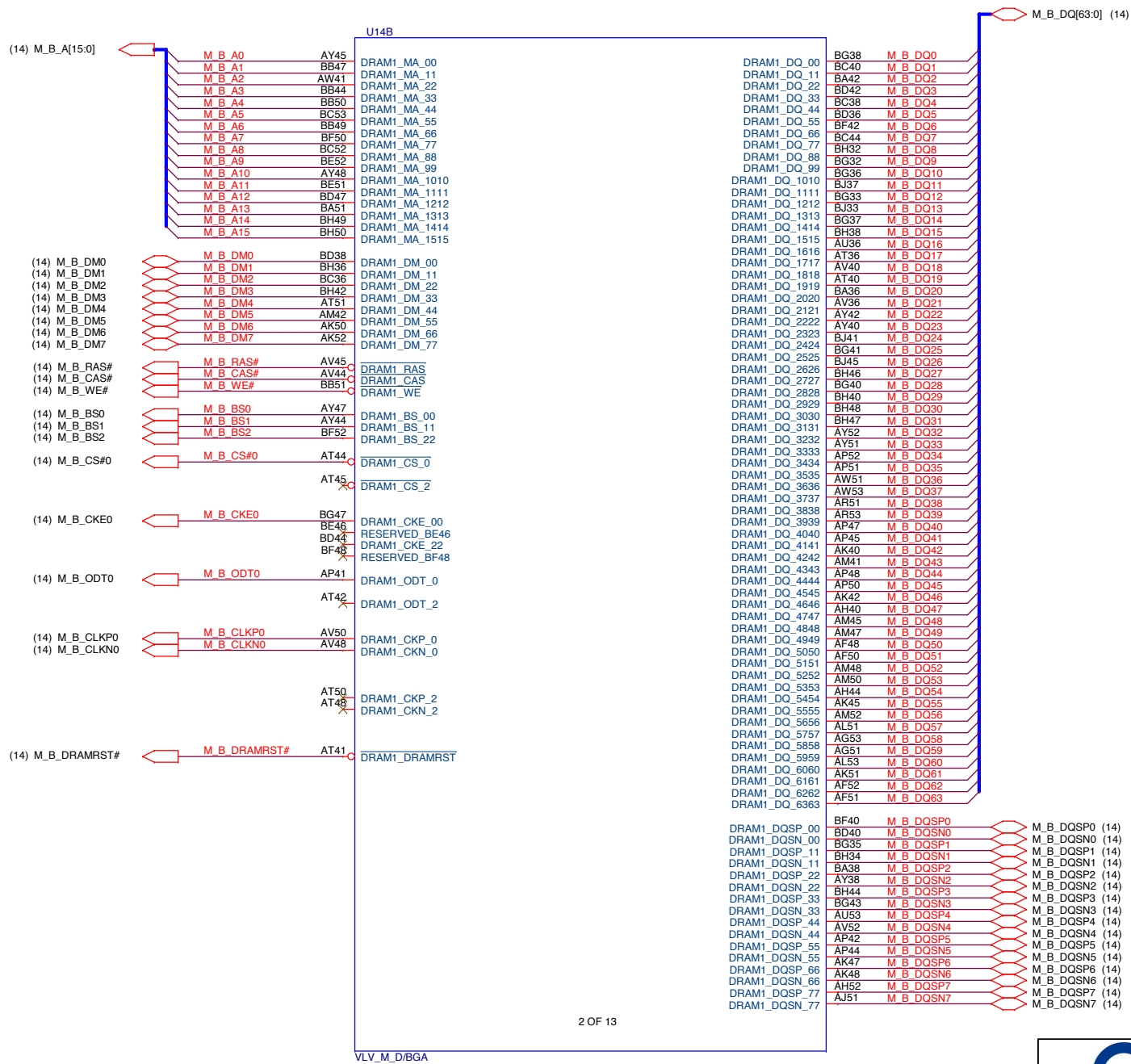
Intel Bay Trail-M Platform Block Diagram

SKUA DC N2820
AJSR1SGUT03 --CPU(1170P)N2820 2.13G SR1SG(FCBGA)STNBSQ



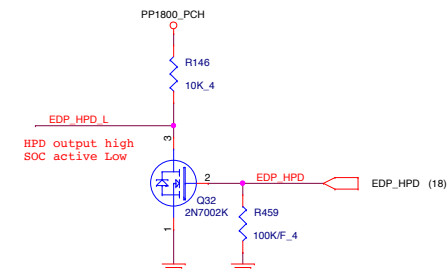
BOM value option:
 SX@ => SOiX
 NSX@=>none SOiX
 HUB@=>USB HUB
 3G@ => LTE
 GD@ =>Google debug





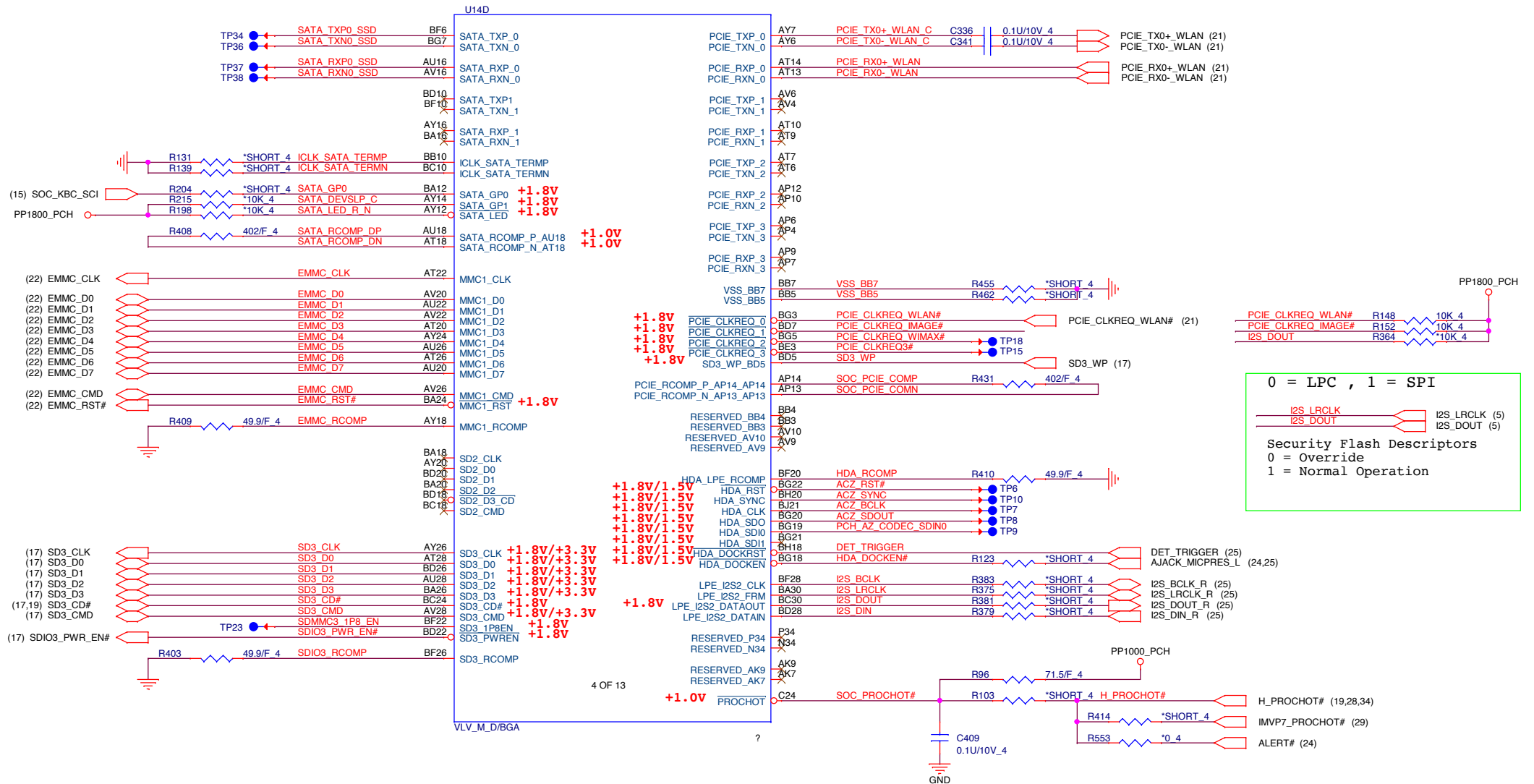
Quanta Computer Inc.
PROJECT : ZHS

Size	Document Number	Rev
	Valley 2/9 (DDR8)	1A
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Pin Name	Strap description	Sampled	Configuration	Note
GPIO_SO_SC_56	Top Swap (A16 Override)	PWROK	0 = Top address bit is unchanged 1 = Top address bit is inverted	
LPE_I2S2_FRM	BIOS Boot Selection	PWROK	0 = LPC 1 = SPI	
GPIO_SO_SC_65	Security Flash Descriptors	PWROK	0 = Override 1 = Normal operation	
DDI0_DDCDATA	DDI0 Detect	PWROK	0 = DDI0 not detected 1 = DDI0 detected	<p>Pull up +1.8V at HDMI side</p>
DDI1_DDCDATA	DDI1 Detect	PWROK	0 = DDI0 not detected 1 = DDI0 detected	
GPIO_SO_NC_13				

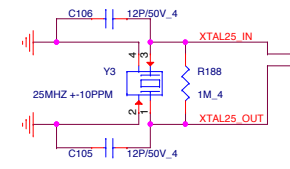
using SoC internal PU



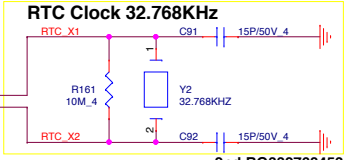
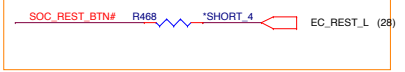
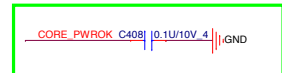
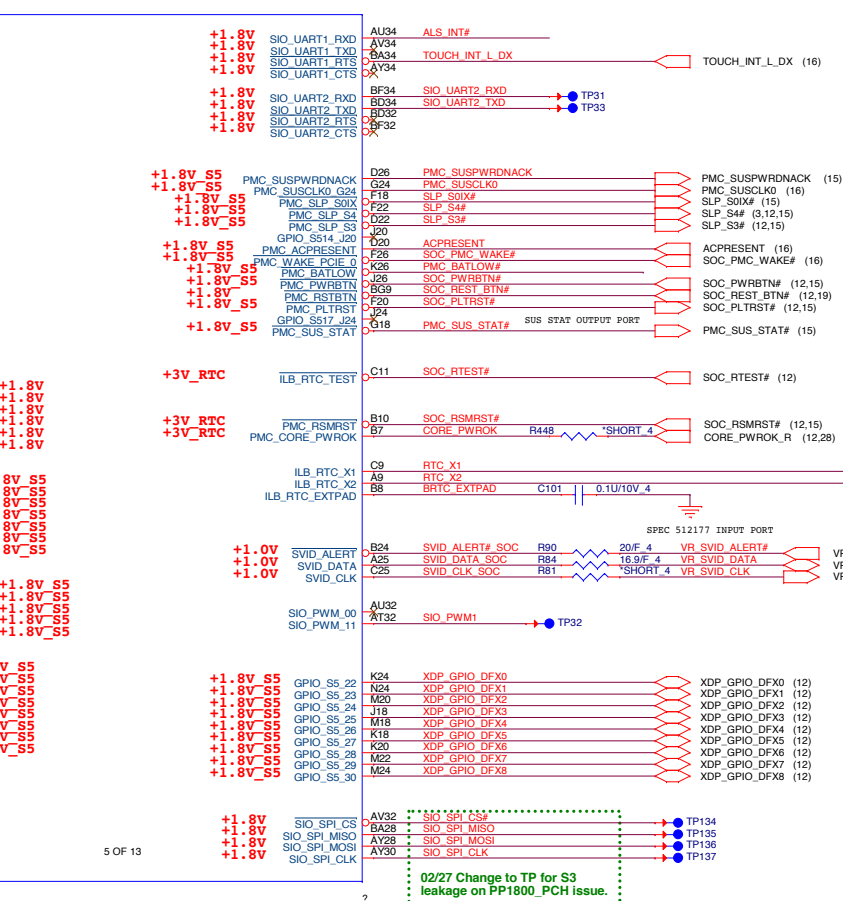
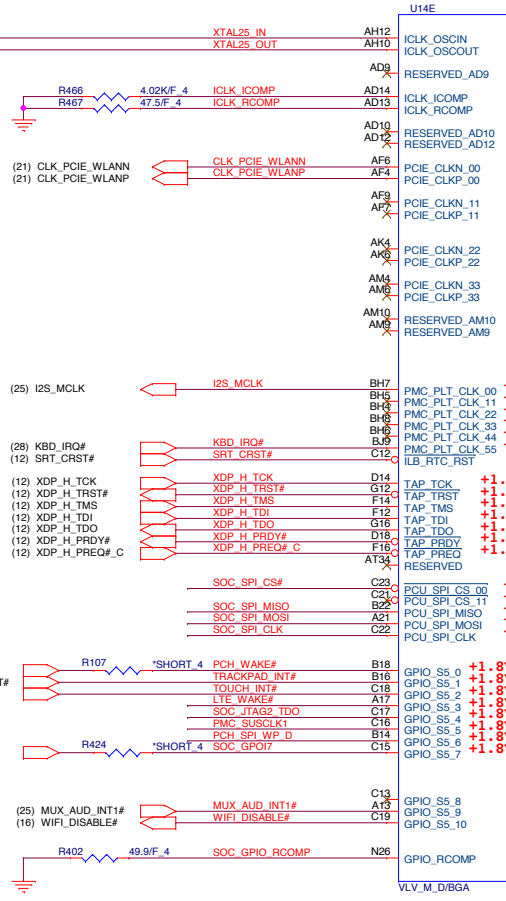
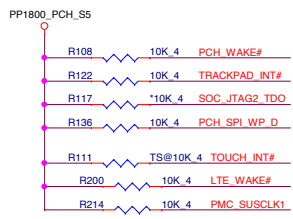
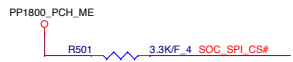
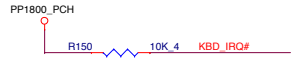
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PROJECT : ZHS

Size	Document Number	Rev
	Valley 4/9 (SD/PCIE/SATA)	1A
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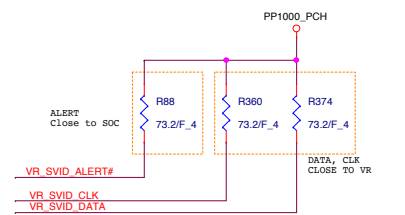
CRYSTAL 25MHZ



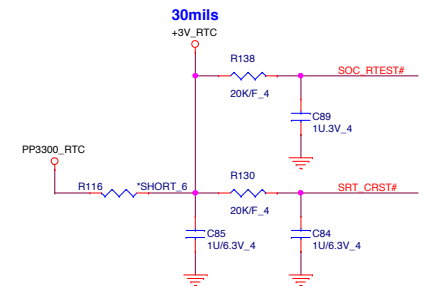
2nd BG625000121(HHE)



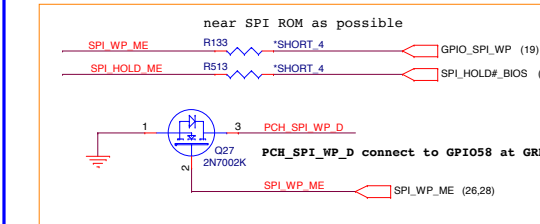
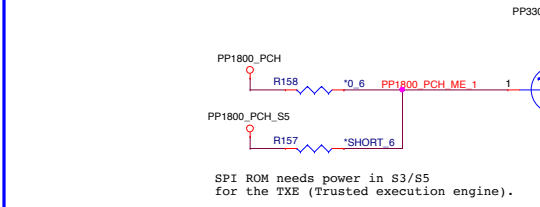
2nd BG332768453



RTC Circuitry(RTC)

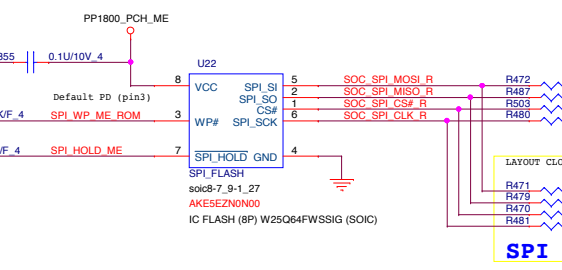


SPI_FLASH

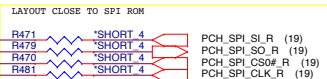


To debug header
To PCH
From Screw/EC

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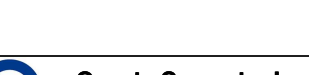
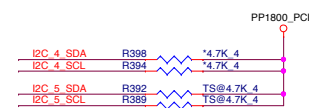
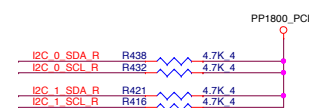
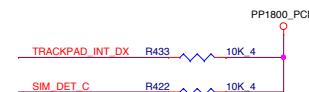
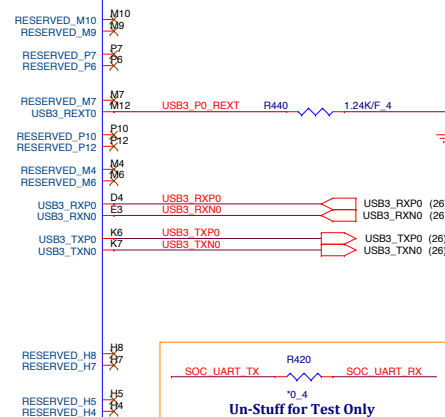
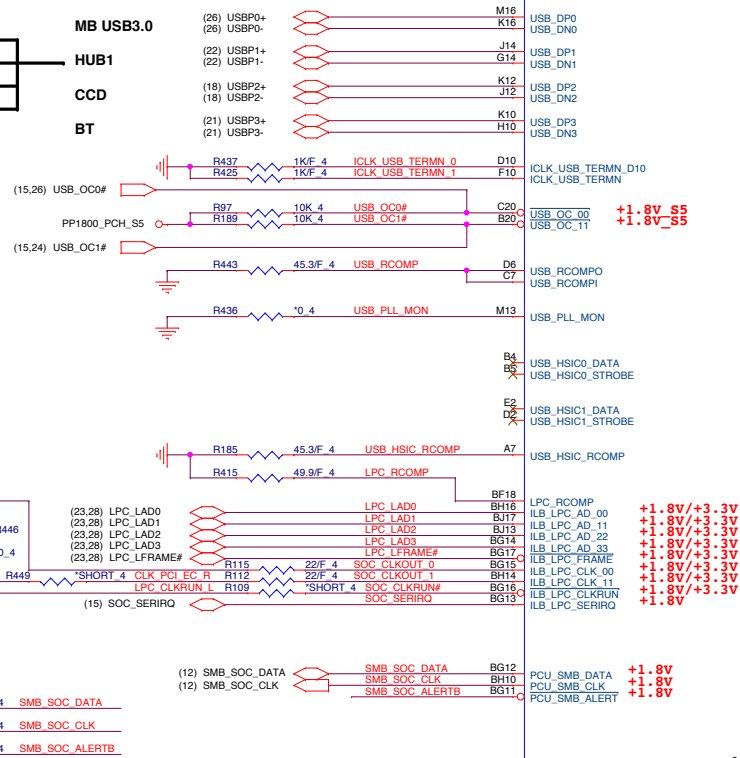
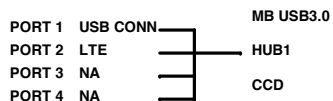
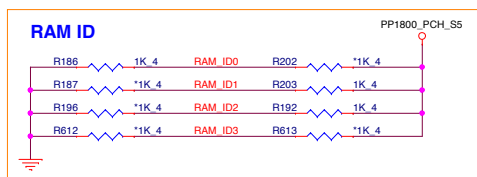


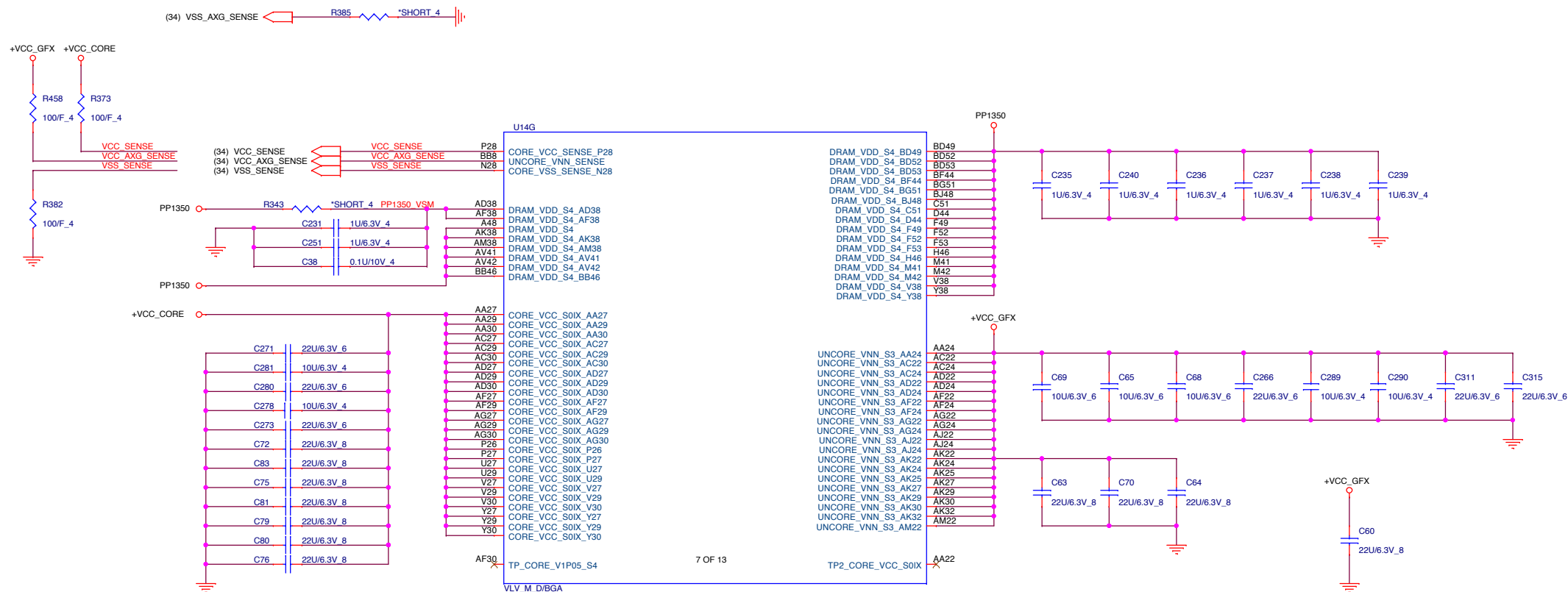
SPI NOR FLASH



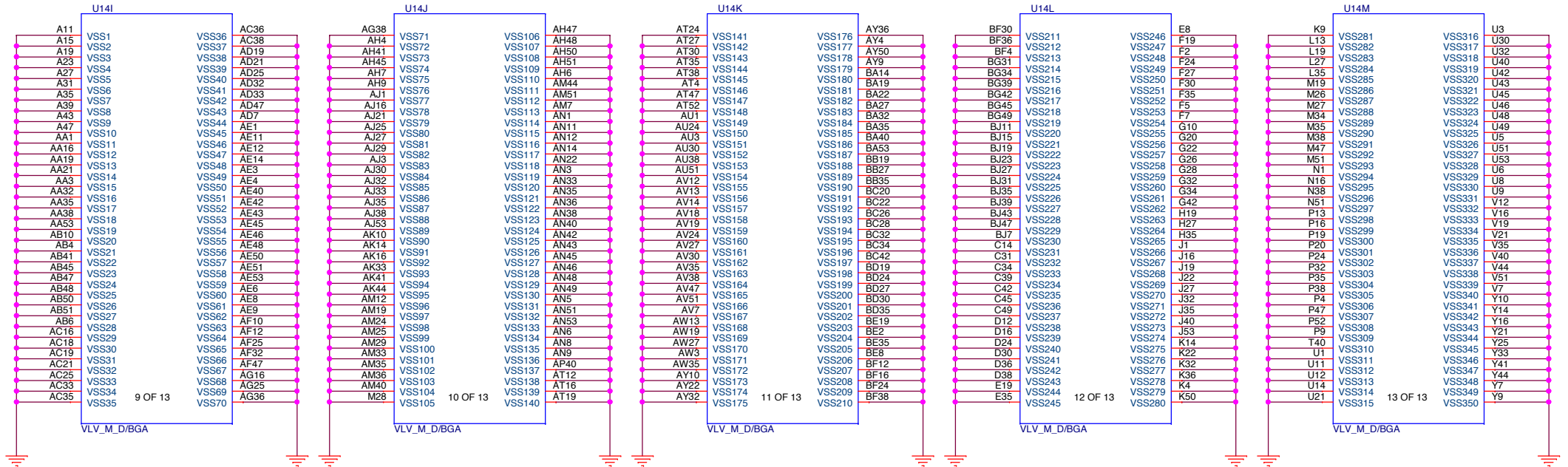
5/19 Update RAM ID for ZHQ and ZHS use.

Vender	RAM ID 210	Q P/N	Mfr. PN	Freq.	Size	Pice
Samsang	0x000	AKD5PGST514	K4B4G1646Q-HYK0	1600MHz	4GB	8
Hynix	0x001	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz	4GB	8
Micron	0x010	AKD5DGSTL07	MT41K128M16JT-125M:K	1600MHz	2GB	8
Hynix	0x011	AKD5PGSTW03	H5TC4G63MFR-PBA	1600MHz	2GB	4
Hynix	0x100	AKD5PGSTW13	H5TC4G63CFR-PBA	1600MHz	2GB	4
Hynix	0x101	AKD5JGETW04	H5TC4G63AFR-PBA	1600MHz	2GB	4
Hynix	0x110	AKD5PGSTW03	H5TC4G63CFR-PBA	1600MHz	4GB	8
Hynix	0x111	AKD5PGSTW03	H5TC4G63MFR-PBA	1600MHz	4GB	8









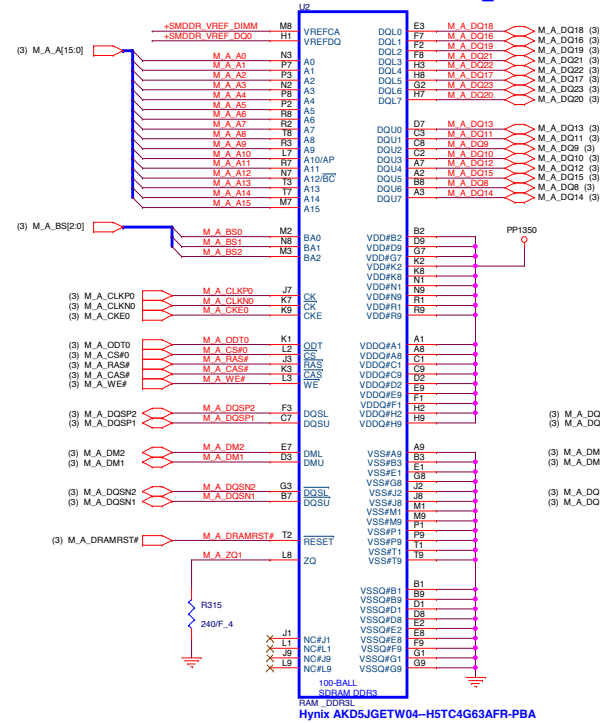
12



Size	Document Number	Rev
	CPU XDP / APS	1A
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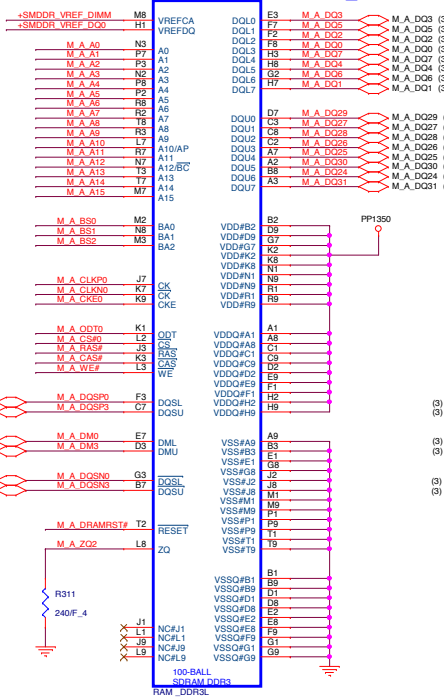
BYTE16_23

BYTE18_15



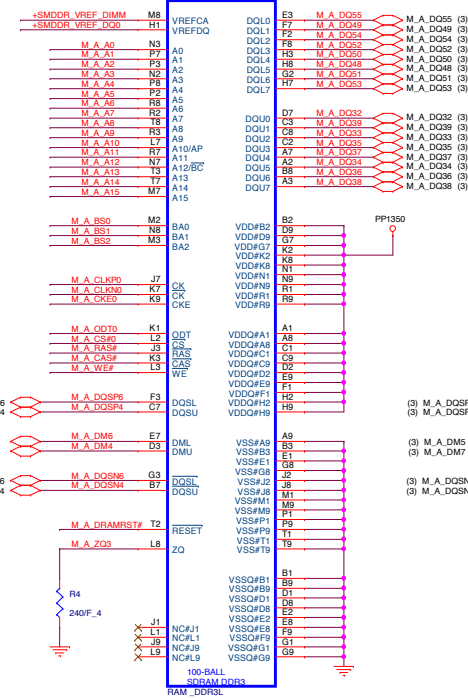
BYTE0_7

BYTE3_24-31



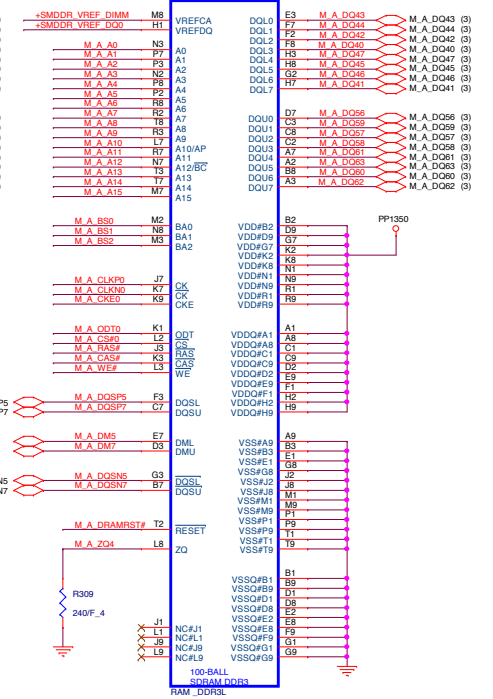
BYTE4_32-39

BYTE6_48-55



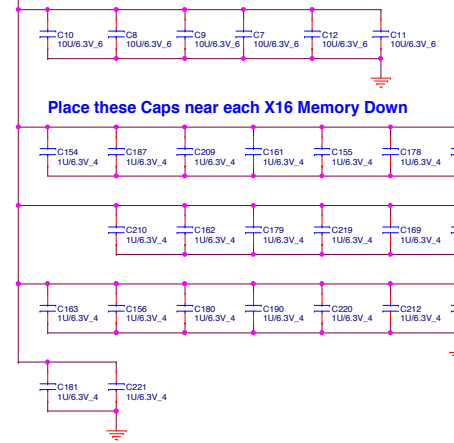
BYTE5_40-47

BYTE7_56-63



Vendor	P/N	
Hynix	AKD5JGETW04	DDR3L 1600MHz 4Gb
Elpida	AKD5JGST400	DDR3L 1333MHz 4Gb
	AKD5JGST404	DDR3L 1600MHz 4Gb

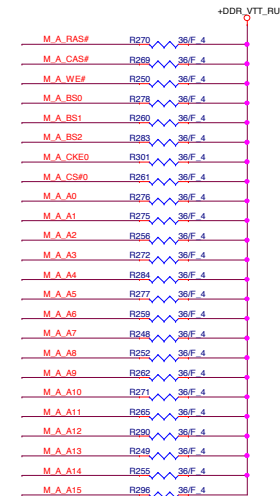
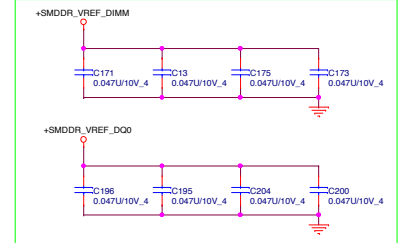
Distributed around all DRAM devices (CHA and CHB)



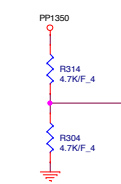
Place these Caps near each X16 Memory Down

C325/C326 are for EMI request

Place these Caps near Memory Down CA & DQ pin



M1 solution



M1 solution



<DDR>

BYTE16_23

BYTE24_31

BYTE0_7

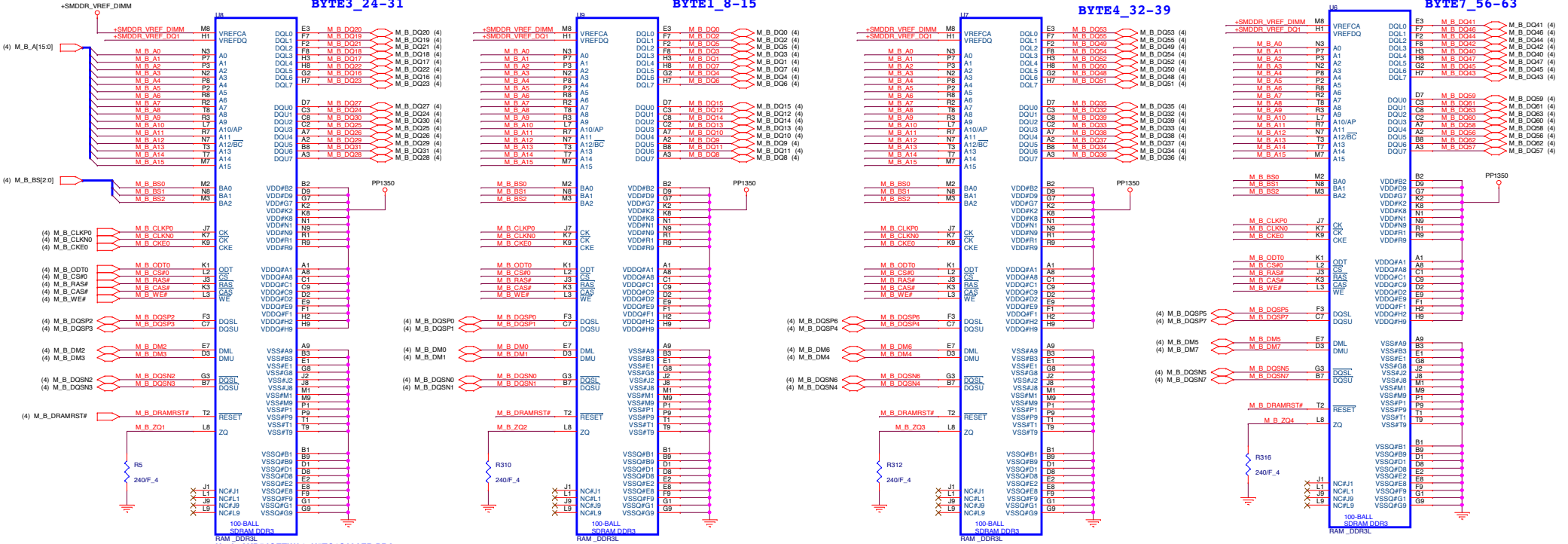
BYTE8_15

BYTE6_48-55

BYTE32-39

BYTE5_40-47

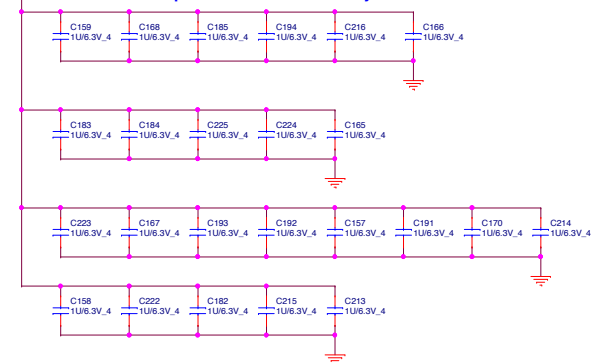
BYTE7_56-63



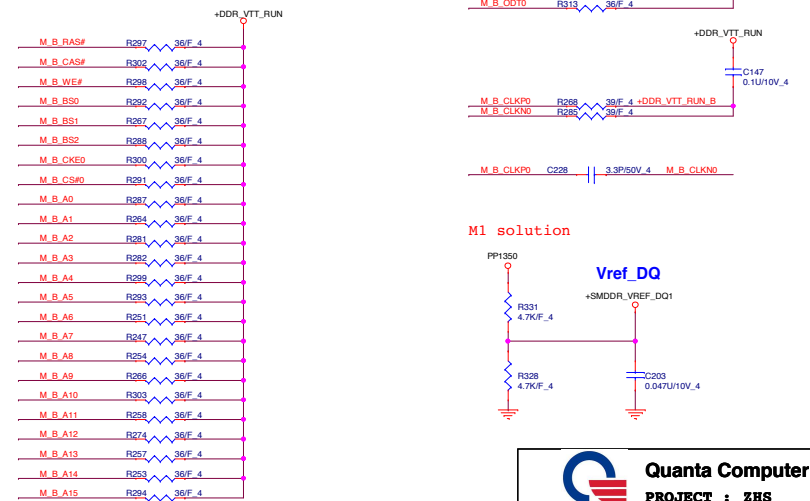
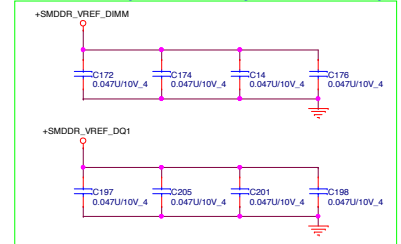
Hynix AKD5JGTW04-H5TCAG63AFR-PBA

Vendor	P/N	
Hynix	AKD5JGTW04	DDR3L 1600MHz 4Gb
Elpida	AKD5JGT400	DDR3L 1333MHz 4Gb
	AKD5JGT404	DDR3L 1333MHz 4Gb

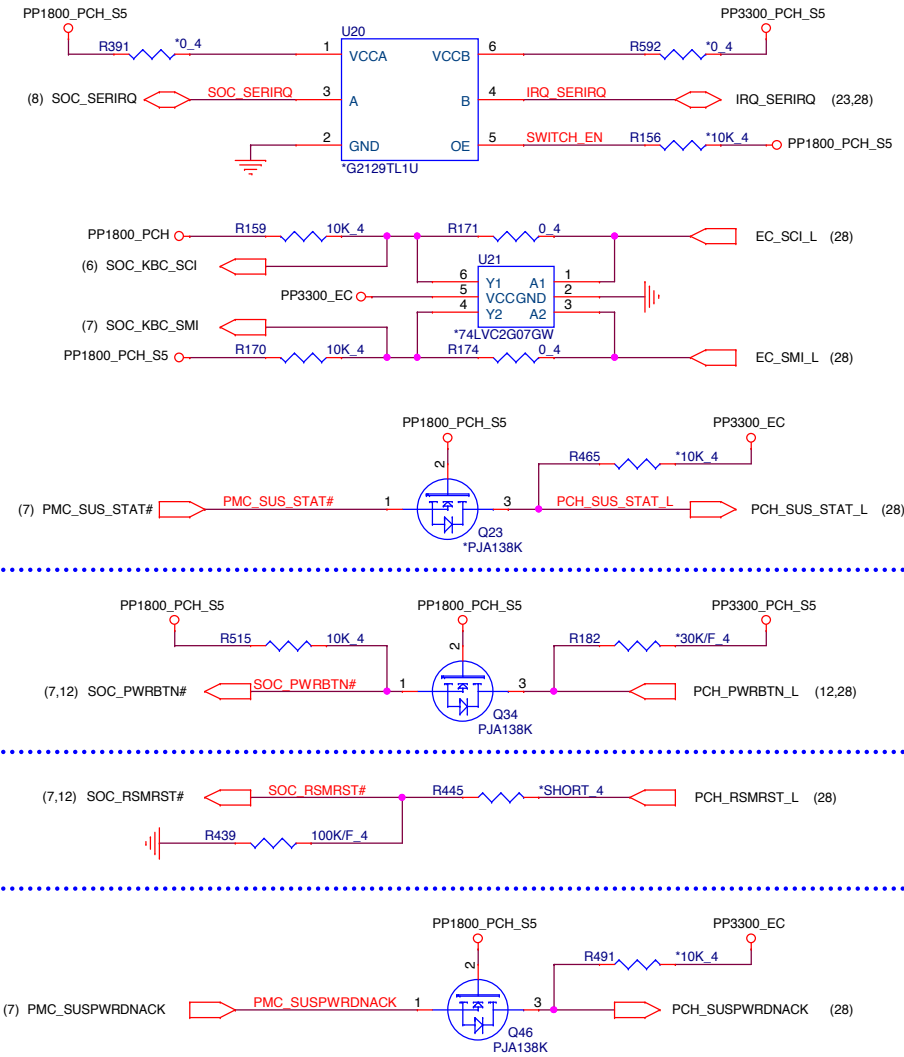
Place these Caps near each X16 Memory Down



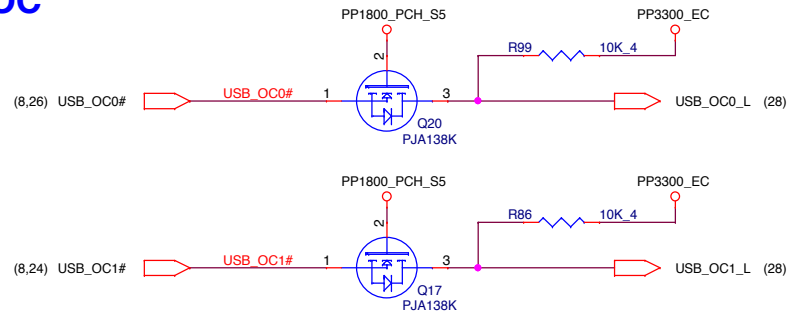
Place these Caps near Memory Down CA & DQ pin



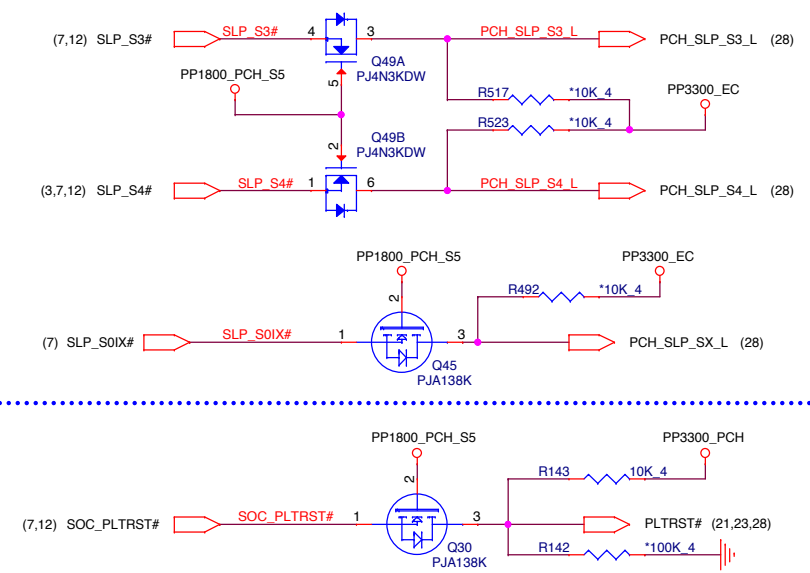
PWRON SEQUENCE



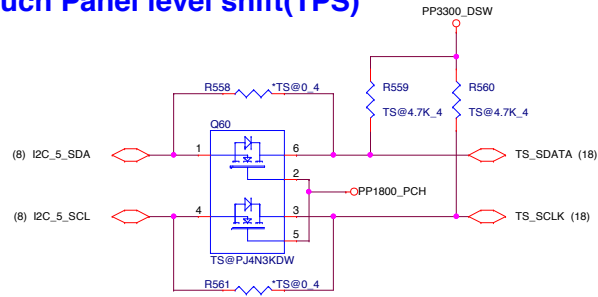
USB OC



PWRON SEQUENCE

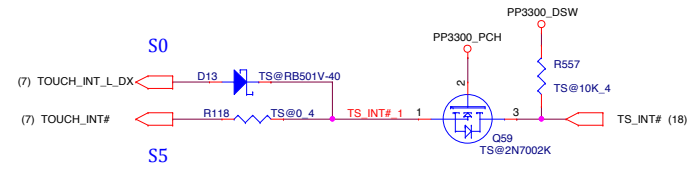


Touch Panel level shift(TPS)

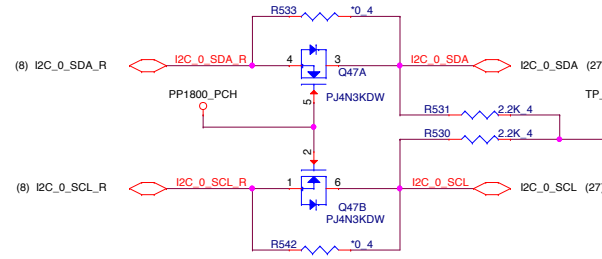


LTE

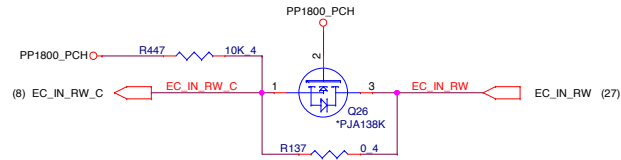
Touch Screen(TPS)



Track Pad

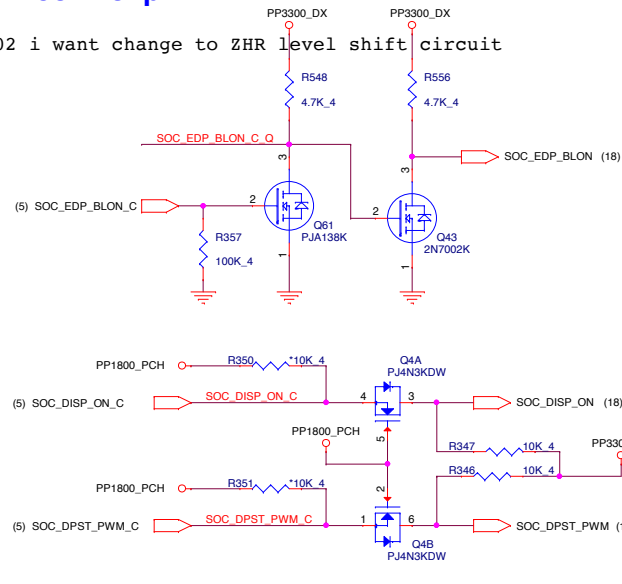


HW RESET

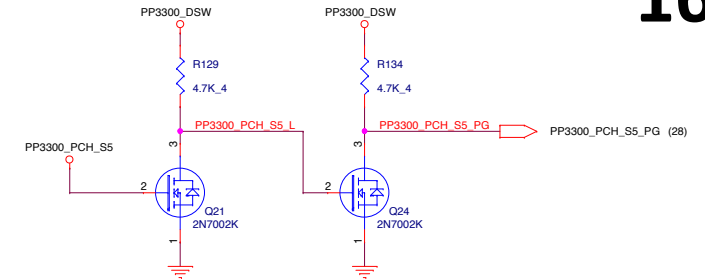


eDP control pin

0402 i want change to ZHR level shift circuit

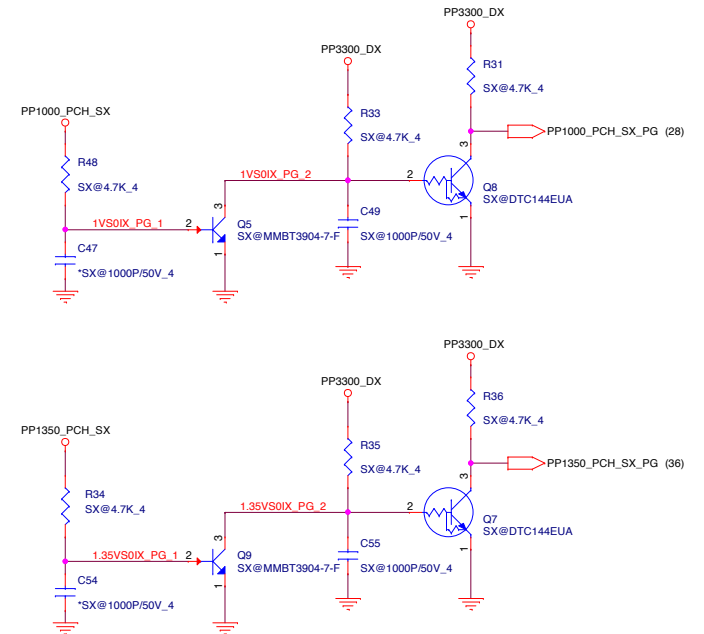


S5 Power Good(+3V_S5)

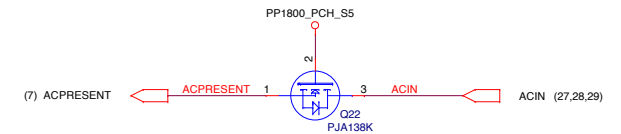


S0iX Power Good

for proto type only, can remove at MP stage if S0ix is not needed



AC Detect



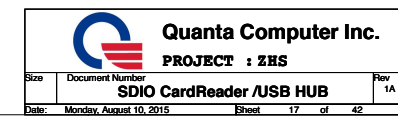
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PROJECT : ZHS

Size	Document Number	Rev
	Level Shifter (SOC_DEV)	1A
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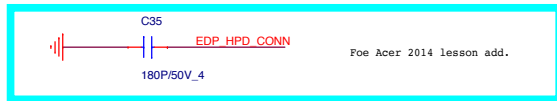
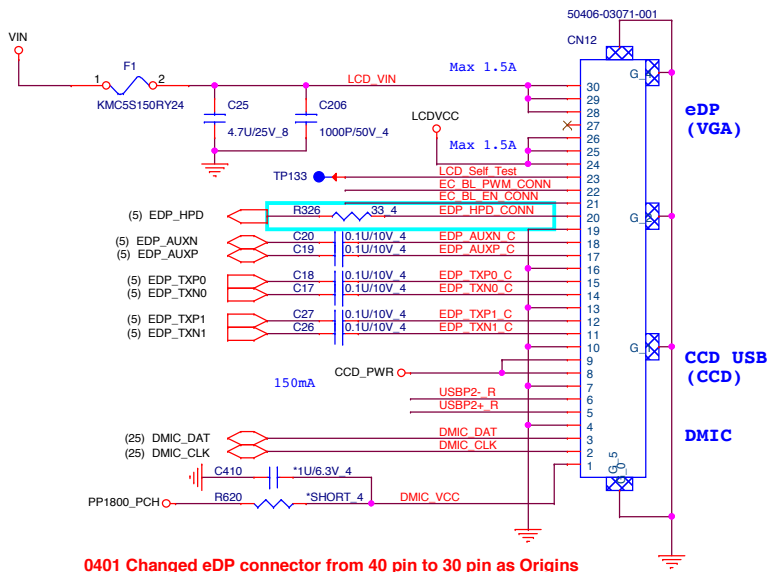
**This is full size SD card
(push-push type)**



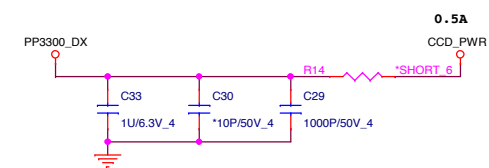
17



LCD CONN



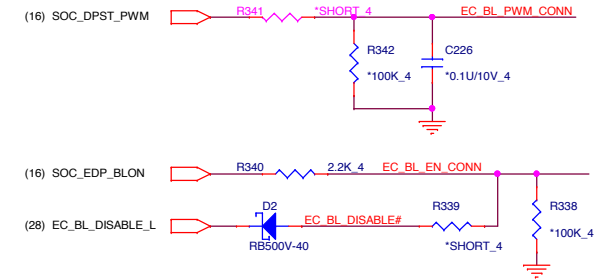
CCD Power(CCD)



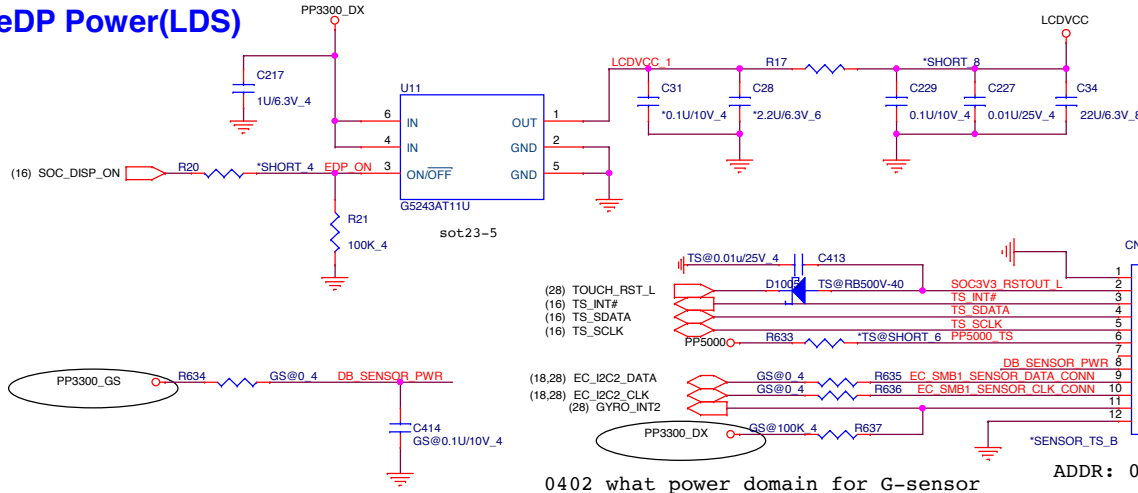
CCD USB(CCD)



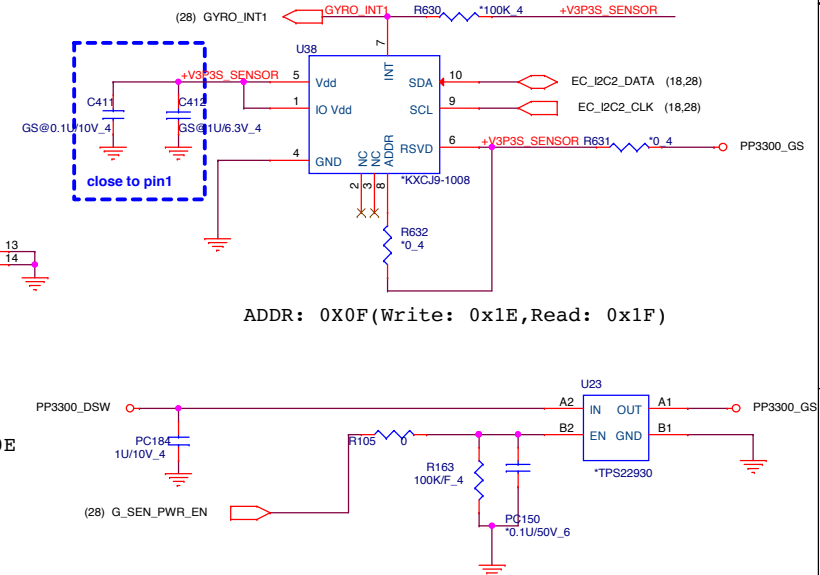
eDP panel control(LDS)



eDP Power(LDS)



0402 added G-sensor / TS-DB



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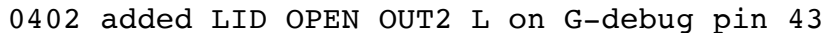
PROJECT : ZHS

LVDS/CCD/TS

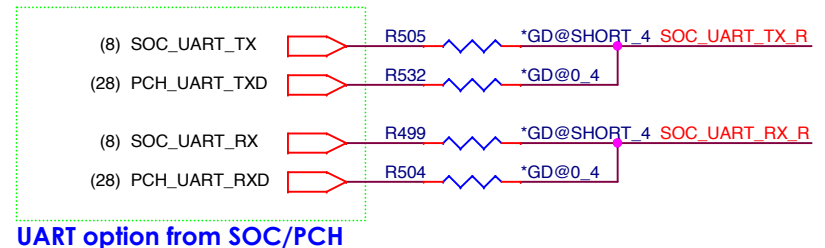
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PIN7	OD	PIN39	OD	PIN49	OD
PIN14	OD	PIN41	OD	PIN50	OD
PIN19	OD	PIN43	OD		
PIN22	OD	PIN44	OD		
PIN28	OD	PIN45	OD		
PIN30	OD	PIN46	OD		
PIN37	OD	PIN47	OD		
PIN38	OD	PIN48	OD		



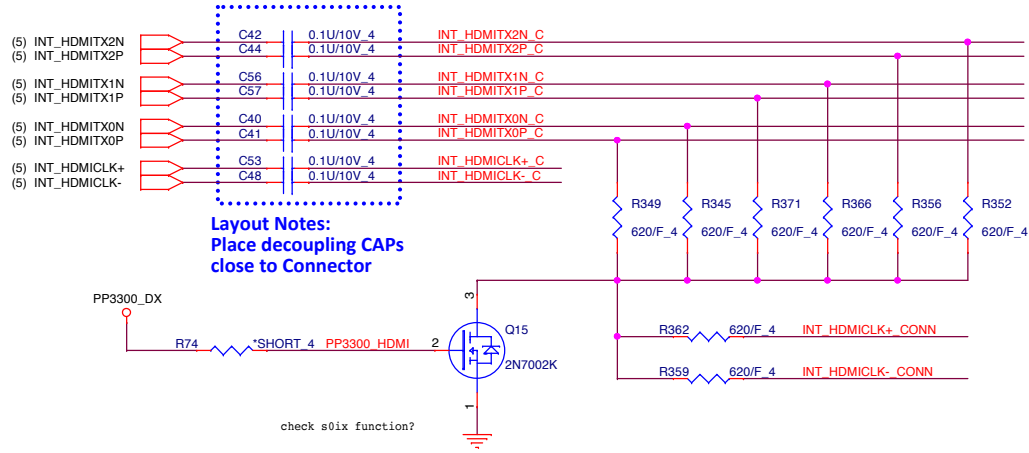
UART(MPC)



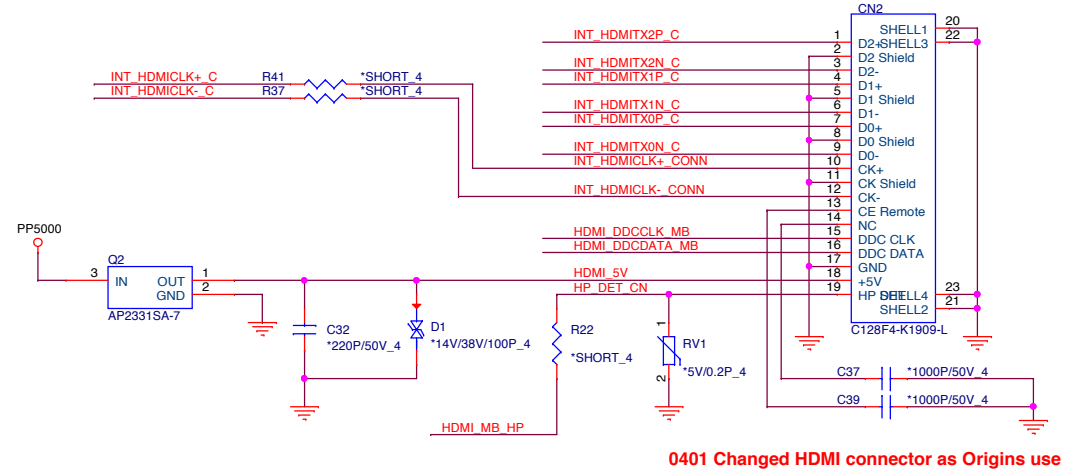
UART Power option



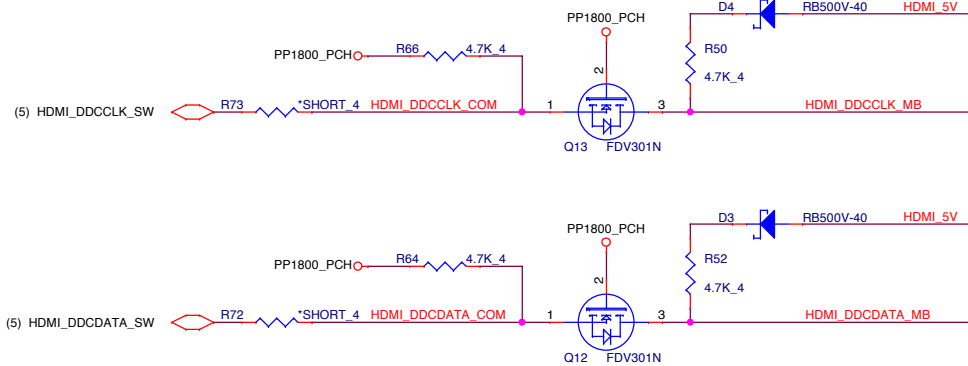
HDMI Cost Reduced level shift (HDM)



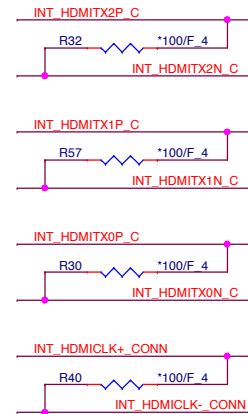
HDMI connector (HDM)



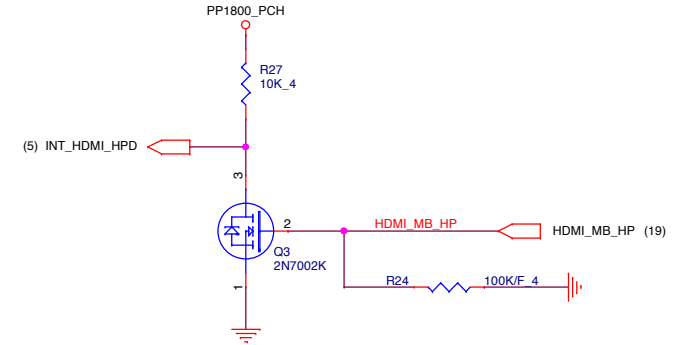
HDMI DDC (HDM)



EMI



HDMI-detect (HDM)



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		1A

HDMI

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WIFI/BT COMBO NGFF E KEY(MNC)

21

(Low Active)
(Low Active)

WLAN OFF L POWER DOWN LAN CHIP from EC?
WIFI_DISABLE_L disable Antenna from PCH?

(16) RF_EN
(28) WLAN_OFF_L
(15,23,28) PLTRST#
(16) WIFI_SUSCLK

TP27
TP26
TP25

NFC_ANT_N
NFC_ANT_P
NFC_VDDANT

PIN54: disable Antenna
PIN52: power down CHIP

RF_EN
PDN#
WLAN_RST#

TP42
TP43

LTE_SOUT
LTE_SIN

TP29
TP1
TP39

NFC_WI_IN
NFC_SWP2_IO
NFC_ACTIVE

NFC Security
WIFI_UART_RX

+WL_VDD

R47 *10K 4 PDN#

TP30
TP3

WIFI_UART_TX
BT_LED

TP129
TP130
TP131
TP132
TP2

PCM_IN
PCM_OUT
PCM_SYNC
PCM_CLK
WLAN_LED1#

+WL_VDD

+WL_VDD

CN16

NGFF

74 3.3Vaux
72 3.3Vaux
70 NC
68 NFC_ANT_N
66 NFC_ANT_P
64 NFC_VDDANT
62 I2C_CLK
60 I2C_DATA
58 W_DISABLE#
56 PDN#
54 PERST0#
52 SUSCLK_32KHz
48 LTE_SOUT
46 LTE_SIN
44 NC
42 NFC_WI_IN
40 NFC_SWP2_IO
38 NFC_ACTIVE
36 NFC Security
34 UART_CTS
32 UART_RTS
UART_Rx

SLOT A-SD

30 KEY
28 KEY
26 KEY
24 KEY

SDIO_RESET
SDIO_WAKE
SDIO_DAT3
SDIO_DAT2
SDIO_DAT1
SDIO_DAT0
SDIO_CMD
SDIO_CLK
GND
USB_D-
USB_D+
GND

23 WIFI_SDIO_RESET
21 WIFI_SDIO_WAKE
19 WIFI_SDIO_DAT3
17 WIFI_SDIO_DAT2
15 WIFI_SDIO_DAT1
13 WIFI_SDIO_DAT0
11 WIFI_SDIO_CMD
9 WIFI_SDIO_CLK
7
5
3
1

TP113
TP114
TP115
TP116
TP117
TP118
TP119
TP120

USBP3- (8)
USBP3+ (8)

BT

75 GND
73 RESERVED
71 RESERVED
69 GND
67 PETn1
65 PETp1
63 GND
61 PERn1
59 PERp1
57 GND
55 PEWake0#
53 CLKREQ0#
51 GND
49 REFCLKN0
47 REFCLKP0
45 GND
43 PETn0
41 PETp0
39 GND
37 PERn0
35 PERp0
33 GND

NFC_NOT_ALLOWED

TP51

WAKE/REQ 53, 55 is OD

WLAN_WAKE_L (16)

CLK_PCIE_WLANN (7)

CLK_PCIE_WLANP (7)

PCIE_RX0-_WLAN (6)

PCIE_RX0+_WLAN (6)

PCIE_TX0-_WLAN (6)

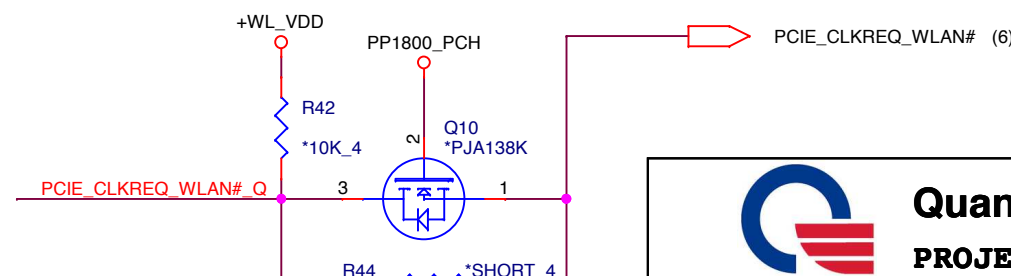
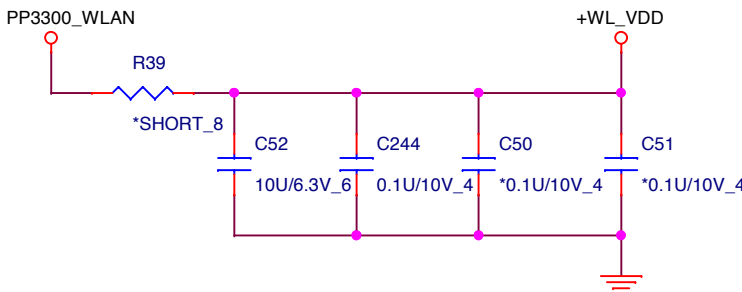
PCIE_TX0+_WLAN (6)

W/L

WLAN_NGFF_CONN(Type 2230)_51745-0750P-005

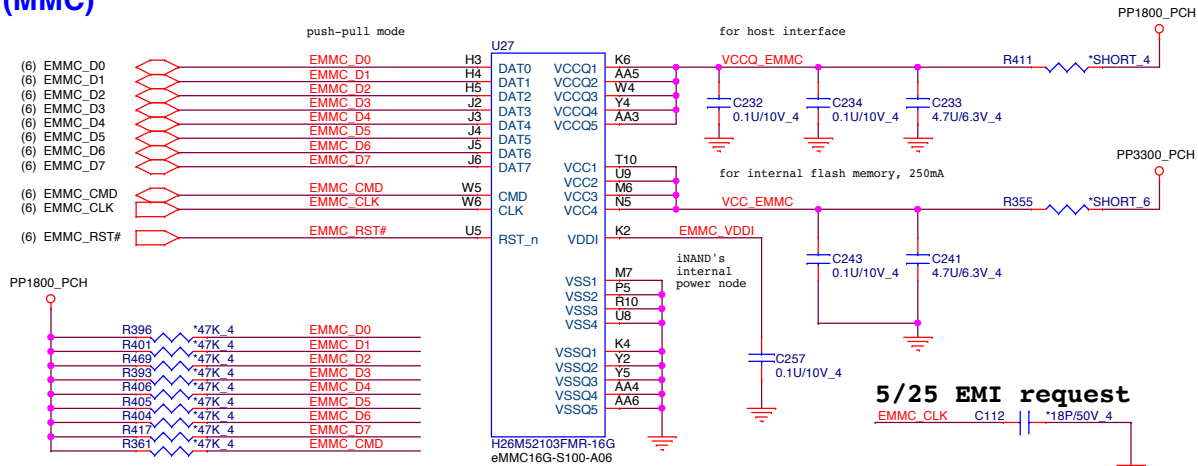
0401 Changed WiFi NGFF connector as Origins use

WL/BT NGFF Power



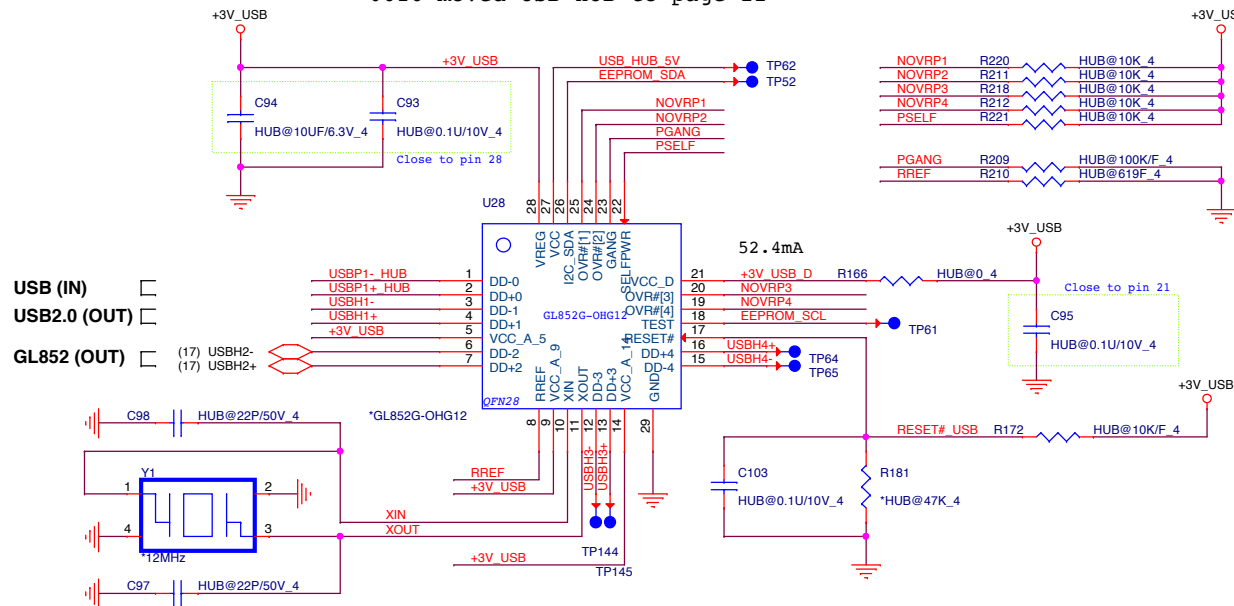
Quanta Computer Inc.
PROJECT : ZHS

EMMC (MMC)

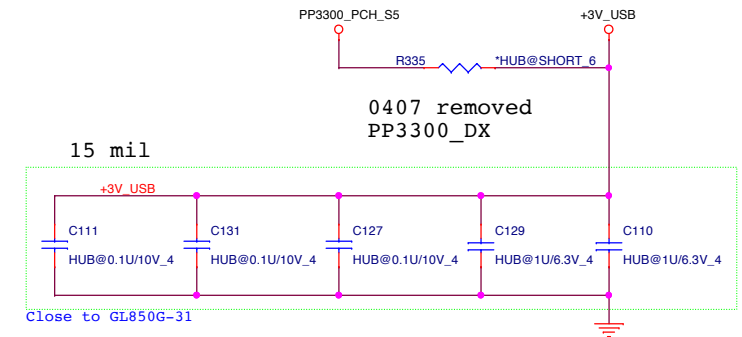


USB HUB (HUB)

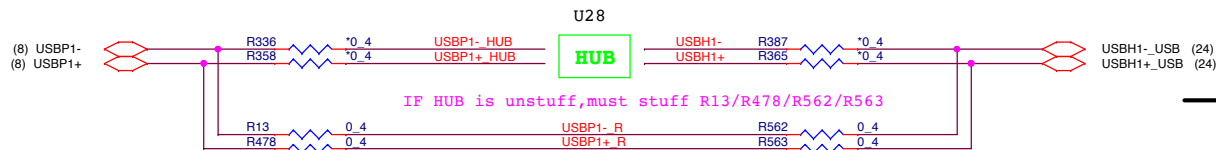
0616 moved USB HUB to page 22



USB HUB power (HUB)

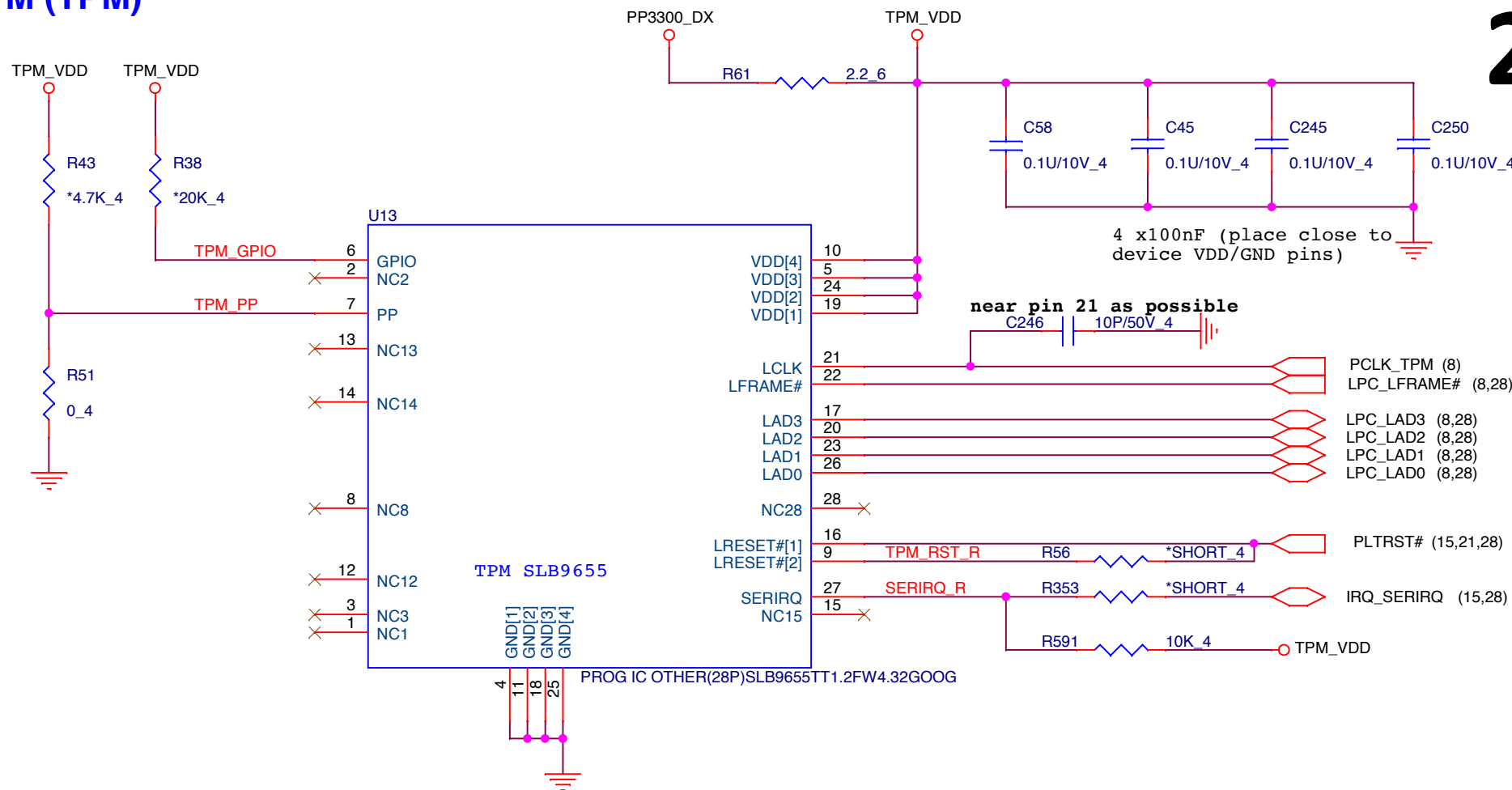


USB option for GL852/USB2.0 (HUB)



TPM (TPM)

23

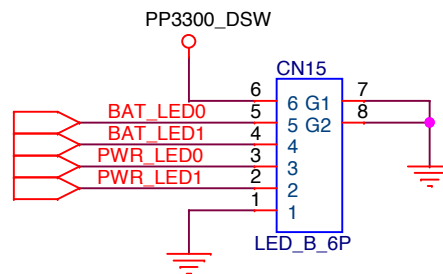


LED board(UIF)

0402 Changed LED board connector as Origins use

BATT_BLUE
BATT_Amber
PWR_Blue
Suspend_Amber

(28) BAT_LED0
(28) BAT_LED1
(28) PWR_LED0
(28) PWR_LED1

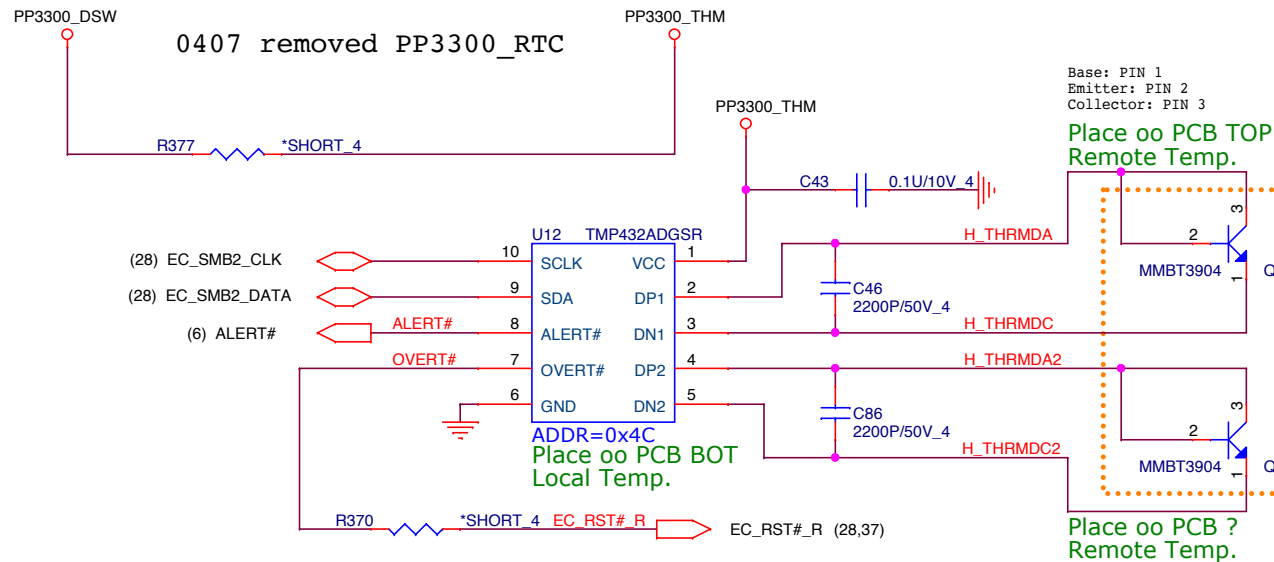


Quanta Computer Inc.

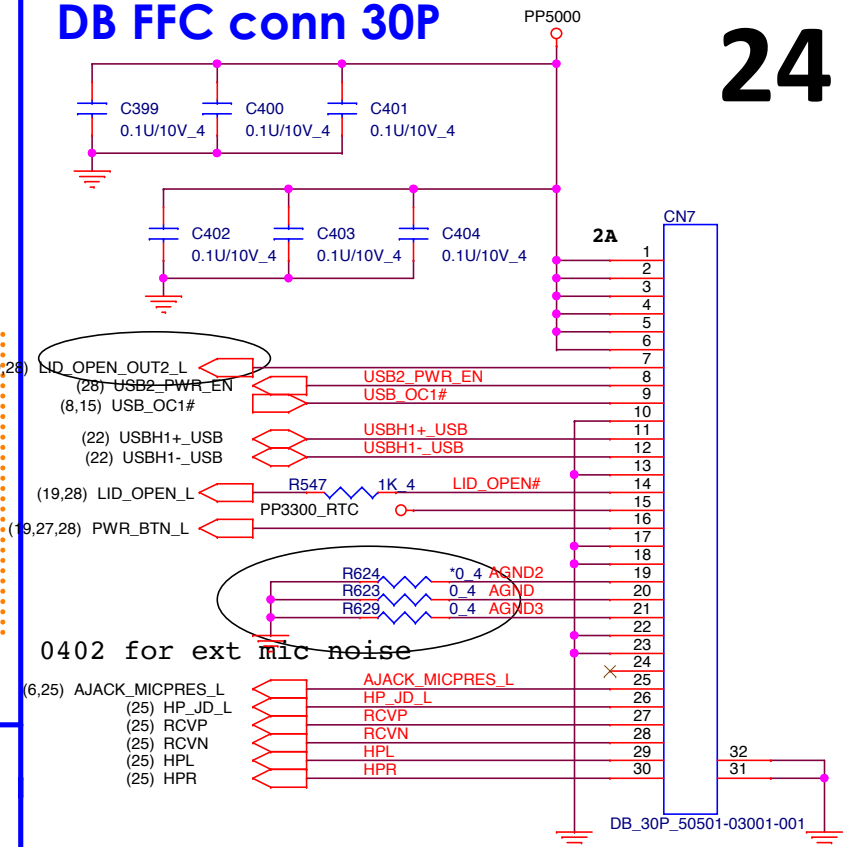
PROJECT : ZHS

Size	Document Number	Rev
	TPM SLB9655 / LED	1A
Date:	Monday, August 10, 2015	Sheet 23 of 42

Thermal Sensor(THM)



DB FFC conn 30P



USB 2.0_ILIM_SEL (USB)

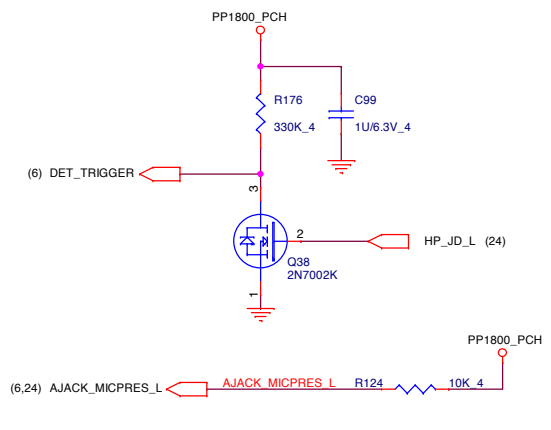
		Quanta Computer Inc. PROJECT : ZHS	
		DB/Thermal sensor/LTE PWR	Rev 1A
Size	Document Number	Date: Monday, August 10, 2015	
Sheet 24 of 42		Rev 1A	

24

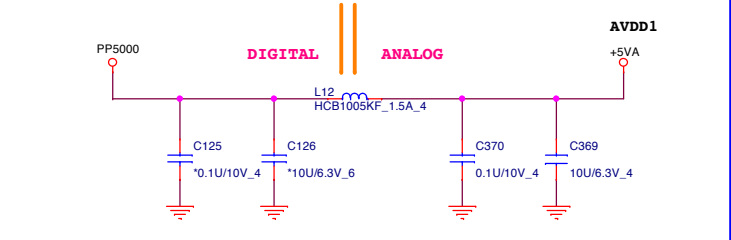
AUDIO CODEC (ADO)

25

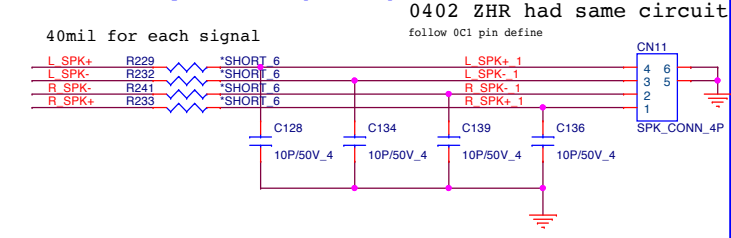
SOC DET (ADO)



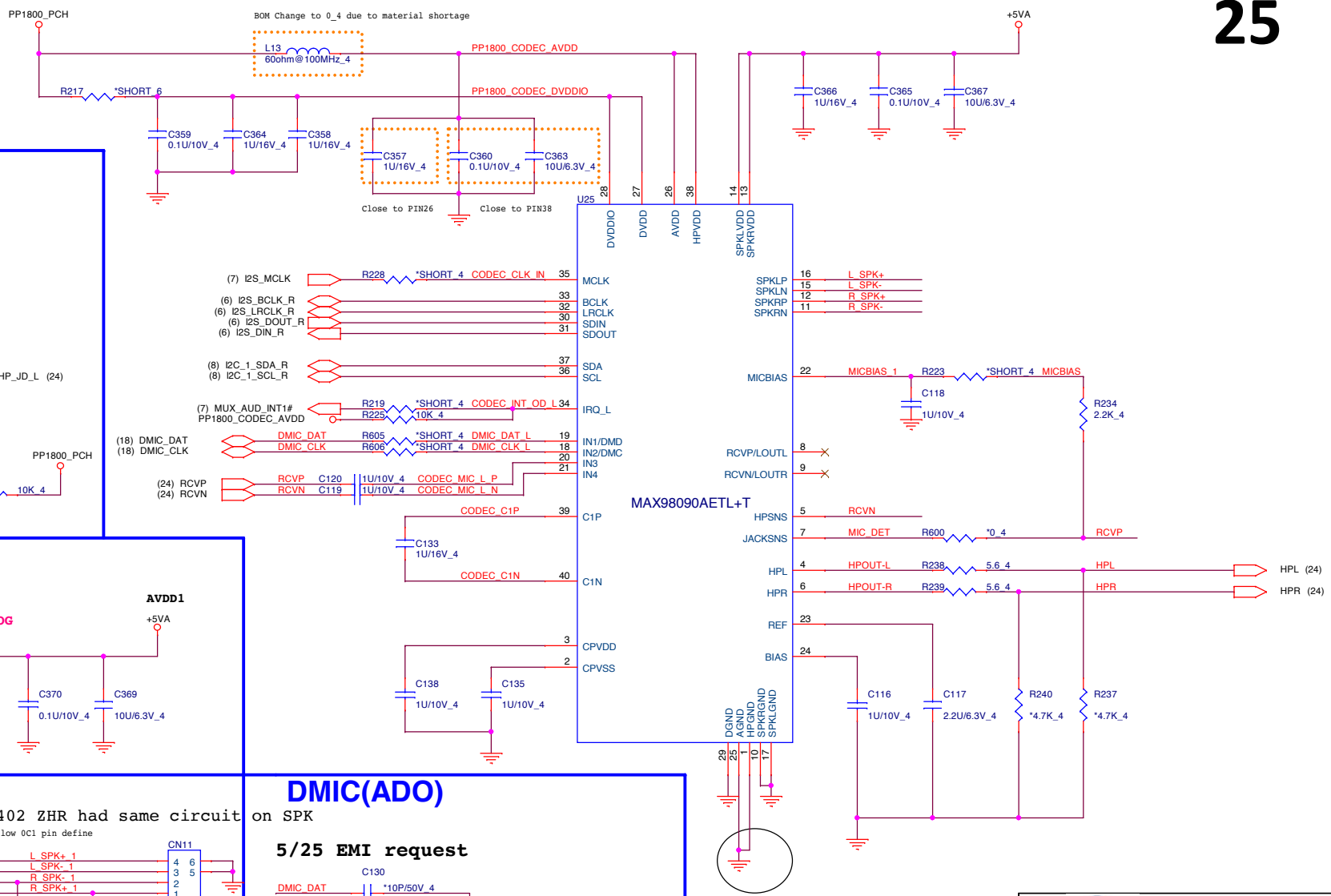
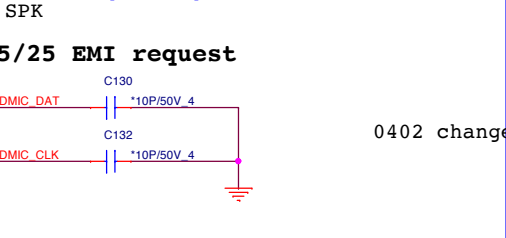
Codec PWR 5V (ADO)



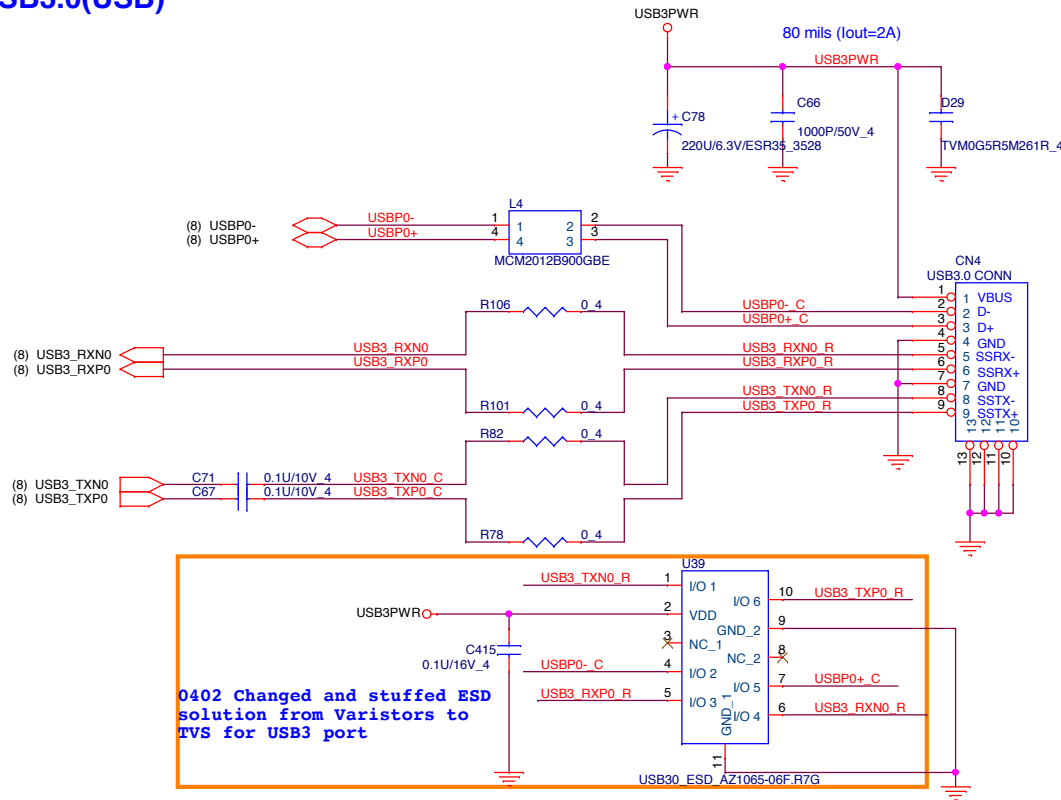
Internal Speaker (ADO)



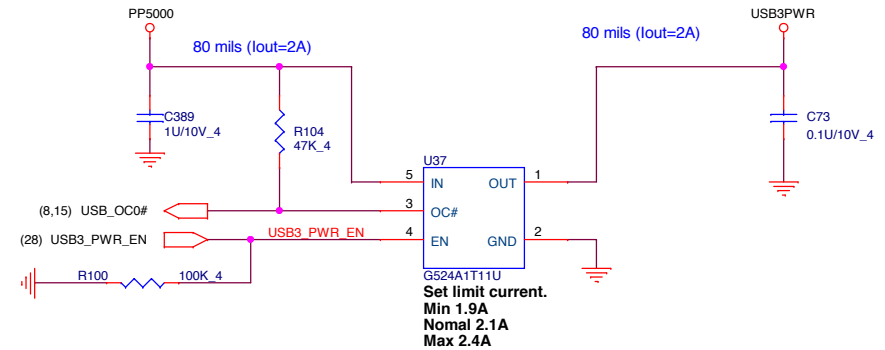
DMIC(ADO)



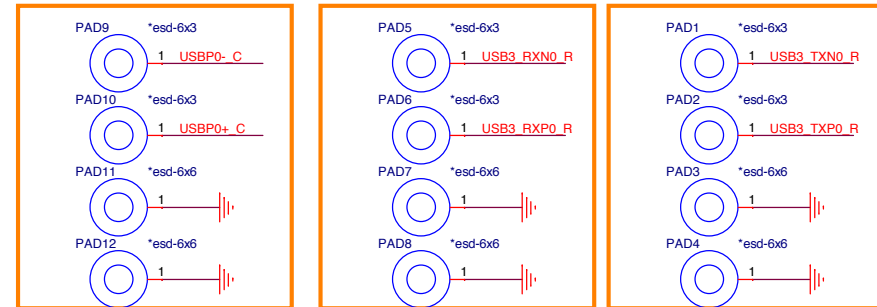
USB3.0(USB)



USB Switch

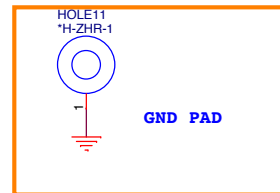
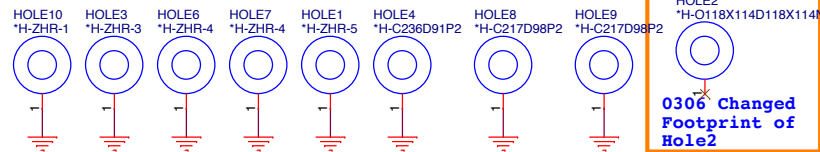
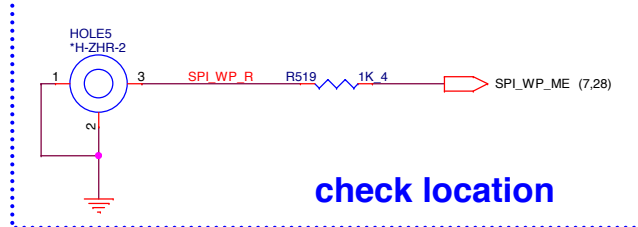


0804 Added PAD1-12
as ESD protection



HOLE(OTH)

ROM WP#



0306 Changed Footprint of Hole2

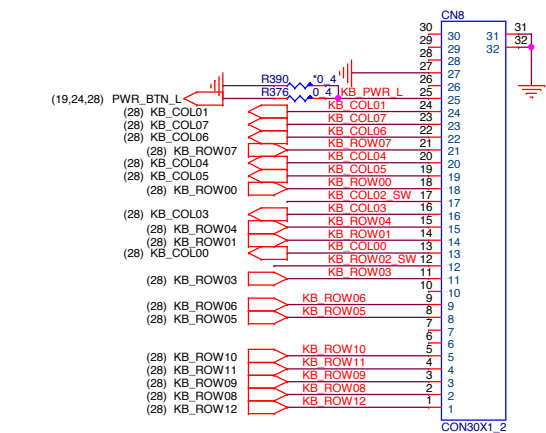


Quanta Computer Inc.

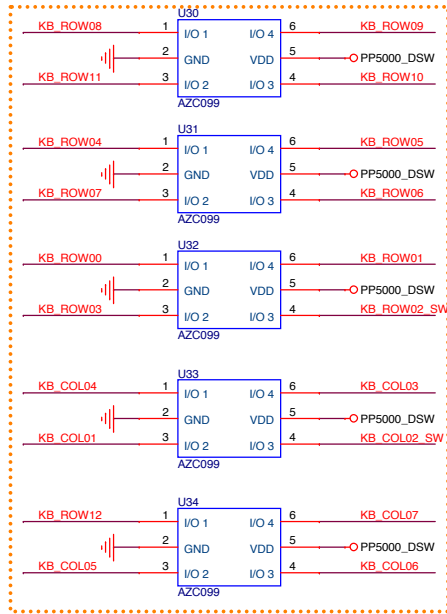
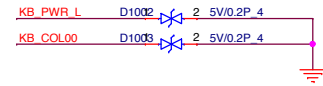
PROJECT : ZHS

Size	Document Number	Rev
	USB3/Hole	1A
Date:	Monday, August 10, 2015	Sheet 26 of 42

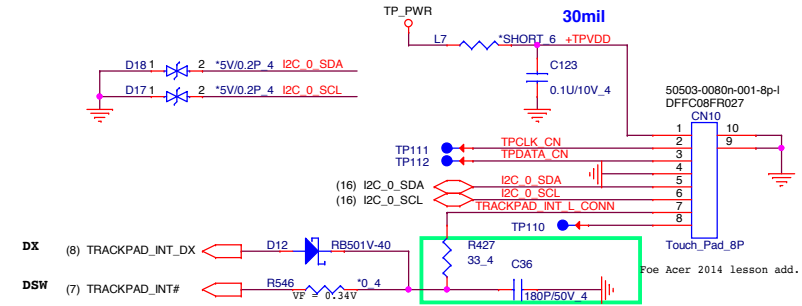
K/B (KBC)



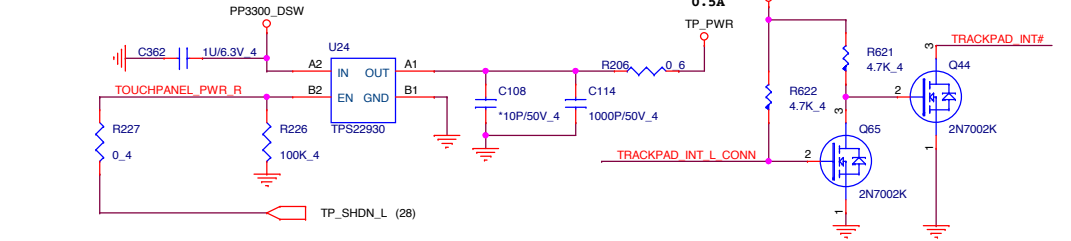
0402 Changed HDMI connector as Origins use



Track PAD BOARD CONN (TPD)

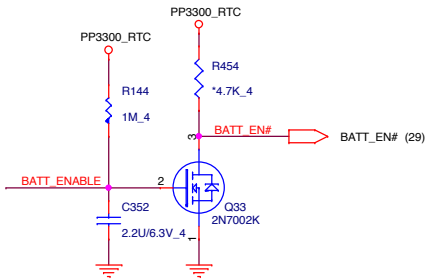


Track PAD Power(TPD)

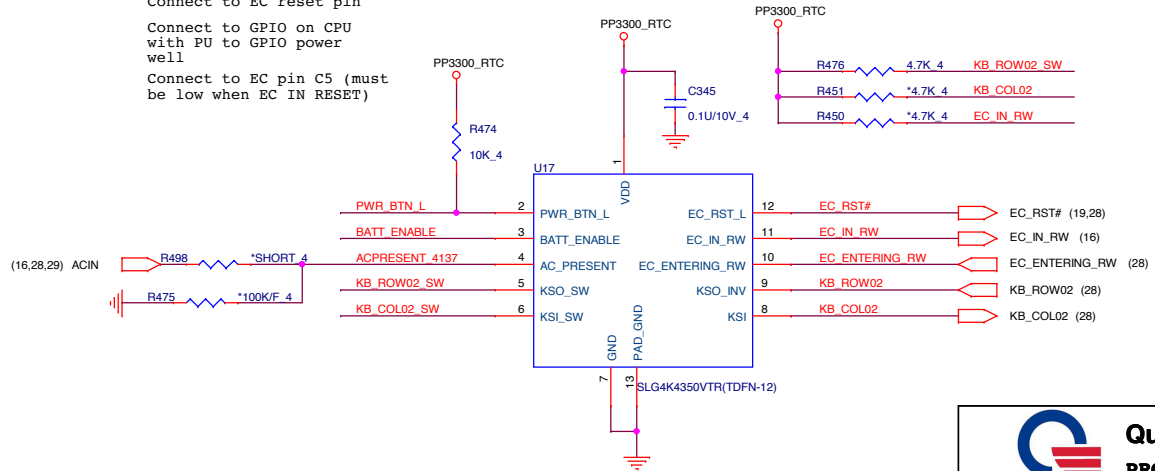


HOLELESS RESET 2-CHIP(KBC)

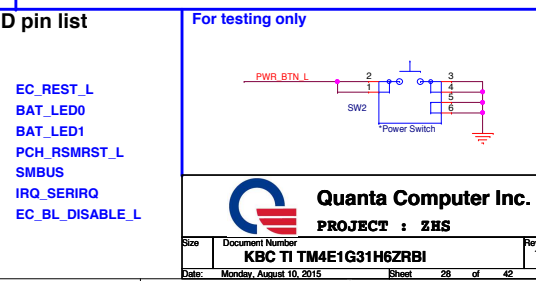
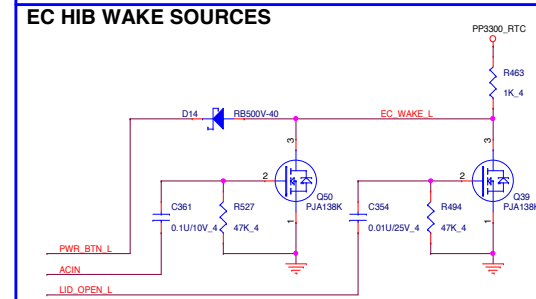
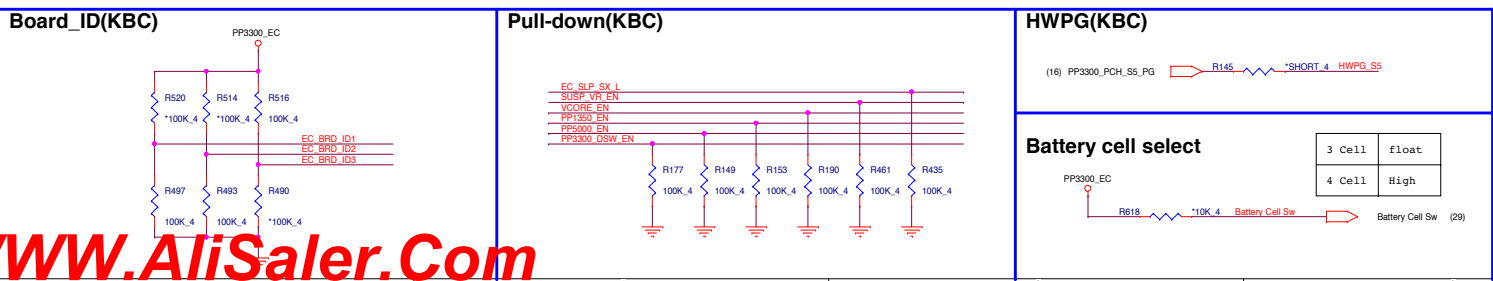
Connect to EC reset pin
Connect to GPIO on CPU
with PU to GPIO power
well
Connect to EC pin C5 (must
be low when EC IN RESET)

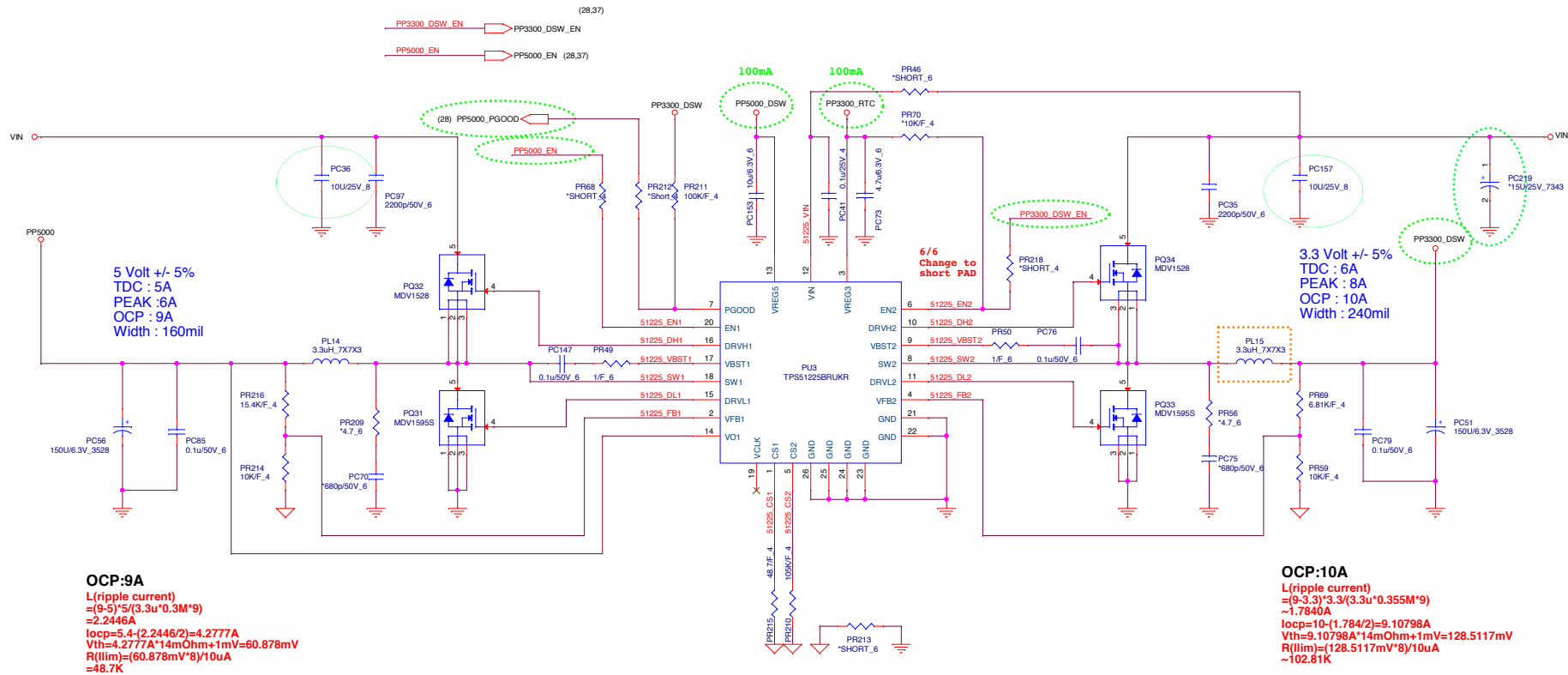


0407 removed SW1



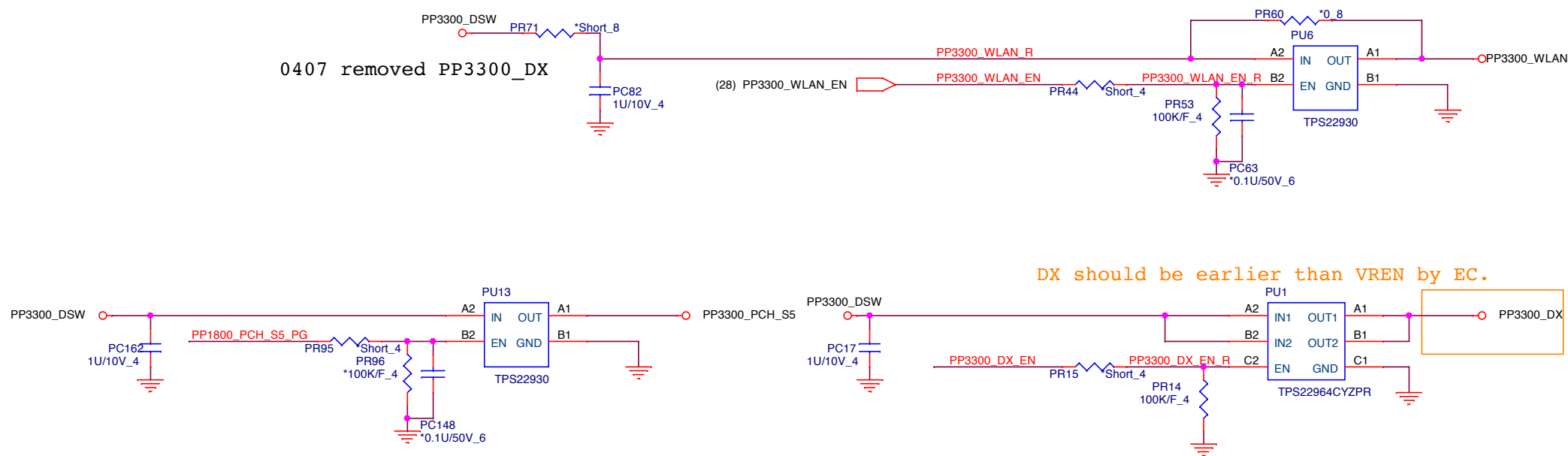
Size	Document Number	Rev
	KB/TP/HW Reset	1A
Date:	Monday, August 10, 2015	Sheet 27 of 42





(36) PP1800_PCH_S5_PG PP1800_PCH_S5_PG
 (28) PP3300_DX_EN PP3300_DX_EN

0407 removed PP3300_DX

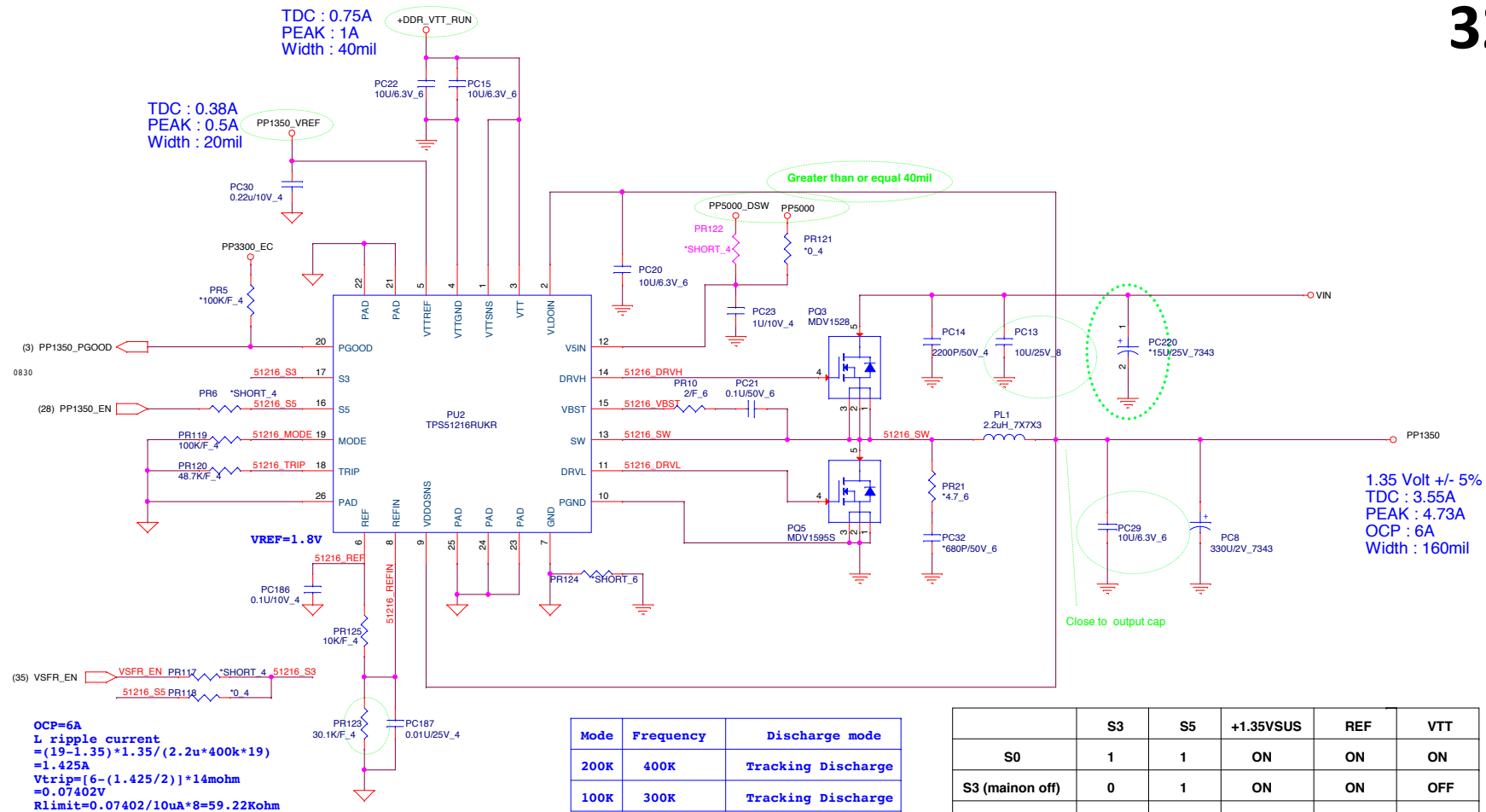


Quanta Computer Inc.

PROJECT :

Size	Document Number	Rev
	Load Switch	1A

Date: Monday, August 10, 2015 Sheet 31 of 42



Quanta Computer Inc.

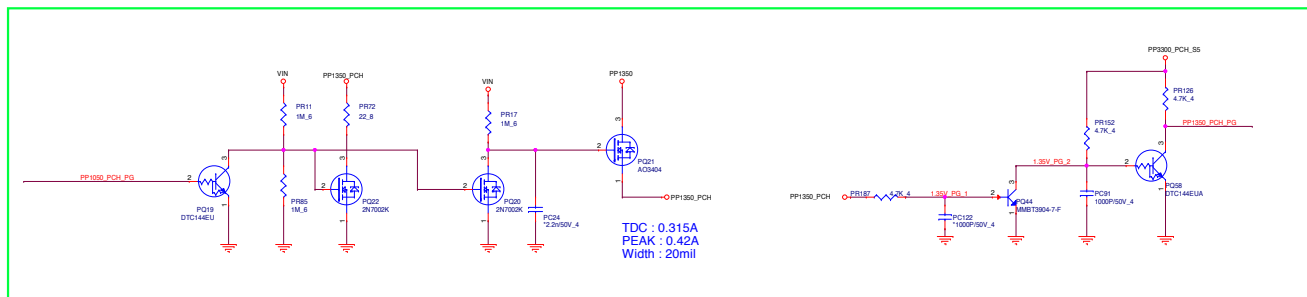
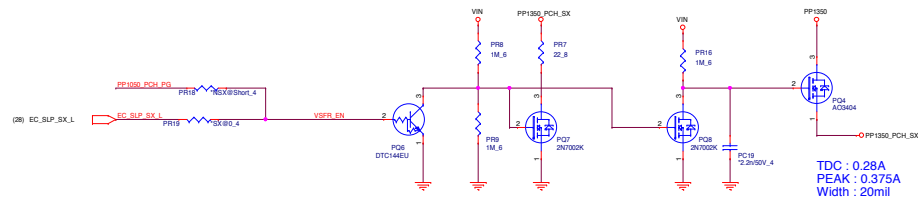
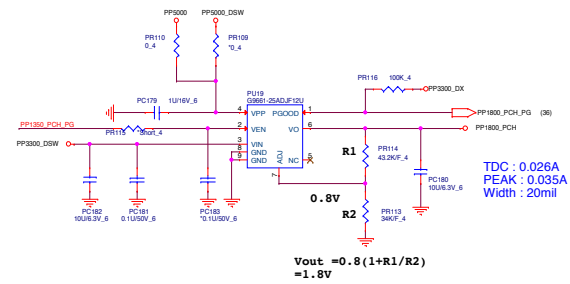
PROJECT :

Size Document Number
DDR 1.35V(TPS51216)
Date: Monday, August 10, 2015 Sheet 32 of 42 Rev 1A

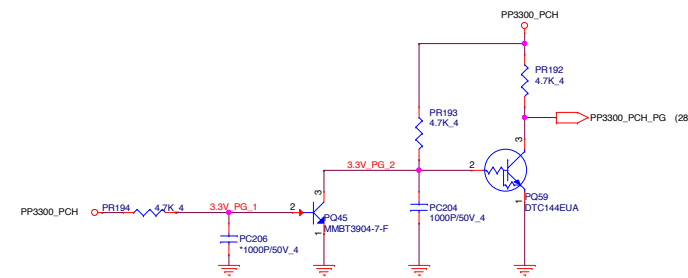
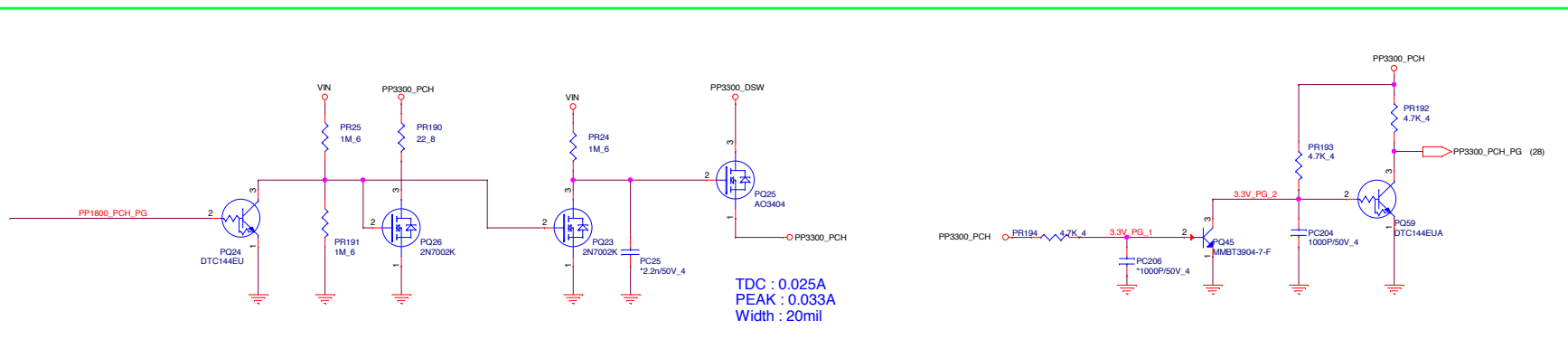
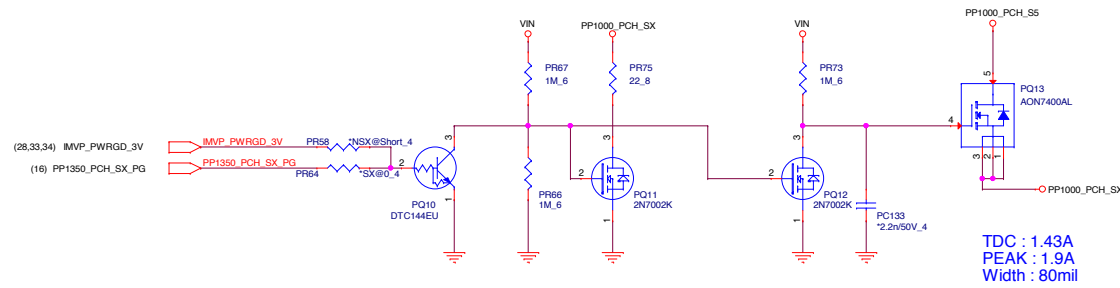
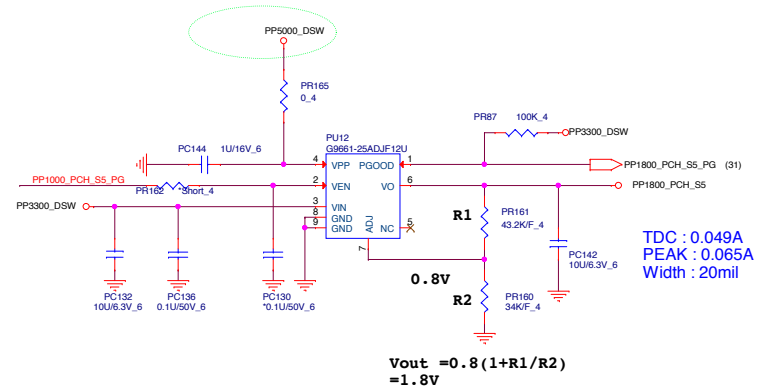
$$V_O = (0.6(R_1 + R_2) / R_2)$$




(32) VSFR_EN
(28,32) SUSP_VR_EN
(28,32) PP1050_PCH_PG



(35) PP1800_PCH_PG
(33) PP1000_PCH_S5_PG





PROJECT : ZHS

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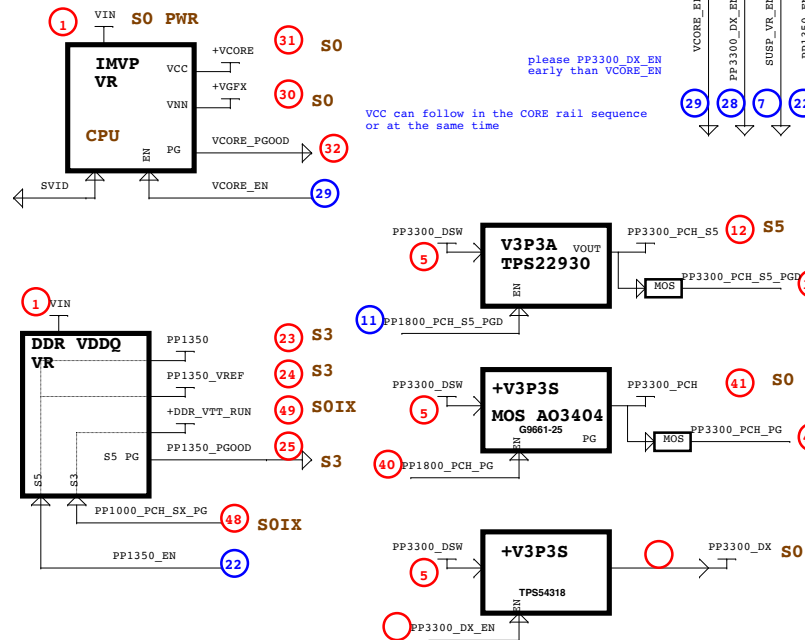


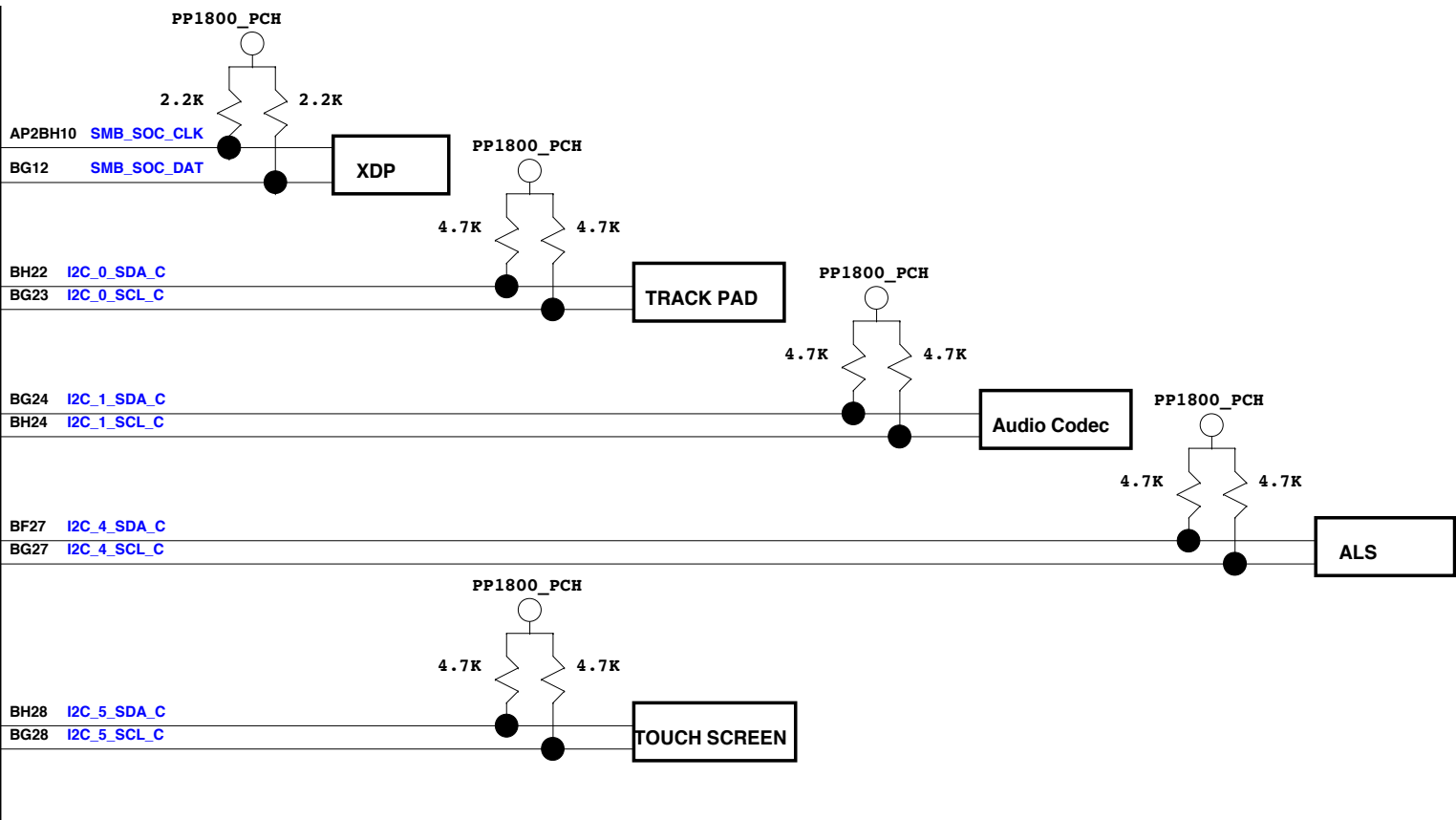
Figure 10 displays the schematic diagrams of the power management ICs for the SOI and SOI+ variants. The diagrams are organized into four quadrants, each showing a different power management block and its connections.

- Top Left (SOI):** Shows the **V1P8A G9661-25** block. Inputs include **PP3300_DSW** (5) and **PP1000_PCH_S5_PGD** (9). Outputs include **PP1800_PCH_S5** (10), **PP1800_PCH_S5_PGD** (11), and **PP1350_PCH_SX_PG** (49). The block is labeled **S5**.
- Top Right (SOI):** Shows the **+VSFR MOS AO3404** block. Inputs include **PP1350** (23) and **EC_SLP_SX_L** (44). Outputs include **PP1350_PCH_SX** (45) and **PP1350_PCH_SX_PG** (49). The block is labeled **SOIX**.
- Bottom Left (SOI):** Shows the **+V1P8S G9661-25** block. Inputs include **PP3300_DSW** (5) and **PP1350_PCH_PG** (38). Outputs include **PP1800_PCH** (39), **PP1800_PCH_PG** (40), and **PP1350_PCH_PG** (38). The block is labeled **S0**.
- Bottom Right (SOI):** Shows the **+V1P35S MOS AO3404** block. Inputs include **PP1350** (23) and **PP1050_PCH_PG** (36). Outputs include **PP1350_PCH** (37), **PP1350_PCH_PG** (38), and **PP1050_PCH_PG** (36). The block is labeled **S0**.
- Top Left (SOI+):** Shows the **V1P0A G9661-25** block. Inputs include **VIN** (1) and **SUSP_VR_EN** (7). Outputs include **PP1000_PCH_S5** (8), **PP1000_PCH_S5_PGD** (9), and **PP1000_PCH** (63). The block is labeled **S5**.
- Top Right (SOI+):** Shows the **+V1P05S TP554318** block. Inputs include **VIN** (1) and **PP1000_PCH_PG** (34). Outputs include **PP1050_PCH** (35), **PP1050_PCH_PG** (36), and **PP1000_PCH_PG** (34). The block is labeled **S0**.
- Bottom Left (SOI+):** Shows the **+V1P0S MOS AO3404** block. Inputs include **PP1000_PCH_S5** (8) and **VCORE_PGOOD** (32). Outputs include **PP1000_PCH** (63), **PP1000_PCH_PG** (34), and **PP1000_PCH** (63). The block is labeled **S0**.
- Bottom Right (SOI+):** Shows the **+V1P0SX MOS AO3404** block. Inputs include **PP1000_PCH** (33) and **PP1350_PCH_SX_PG** (46). Outputs include **PP1000_PCH_SX** (47), **PP1000_PCH_SX_PG** (48), and **PP1000_PCH_SX_PG** (48). The block is labeled **SOIX**.

SMBUS

Bay-trail M

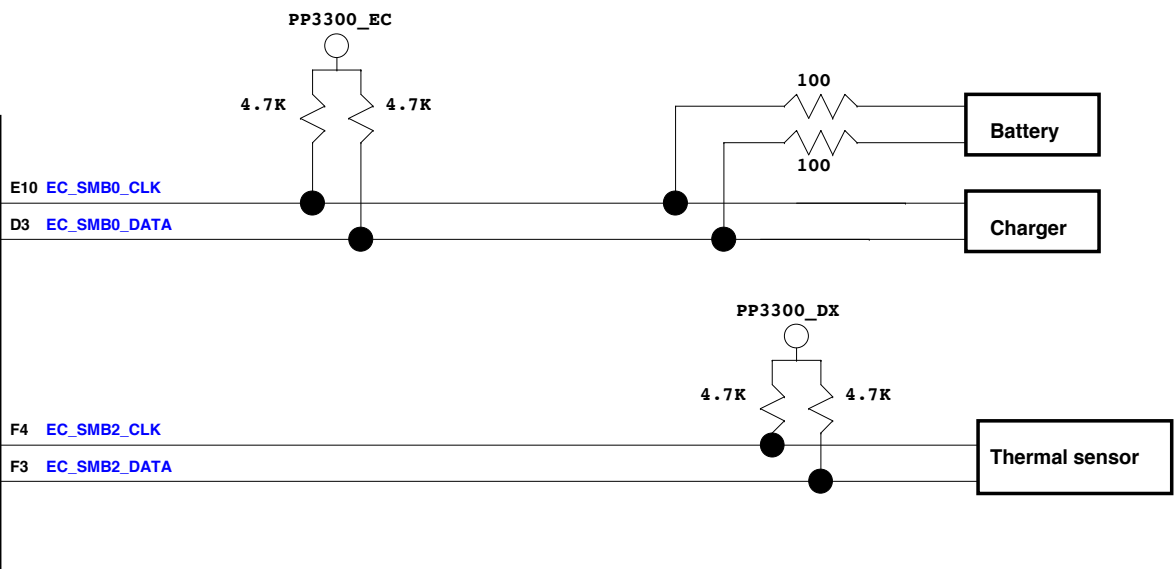
I2C



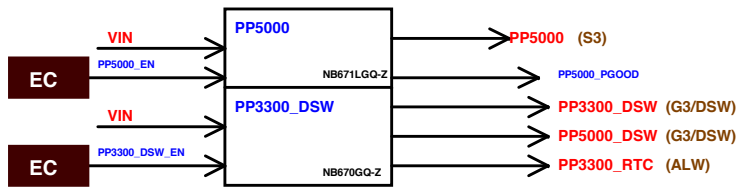
KBC

TI

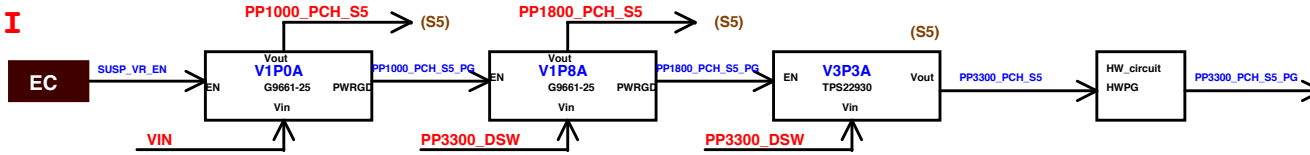
SMBUS



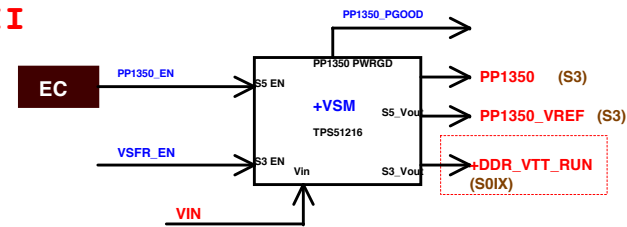
I



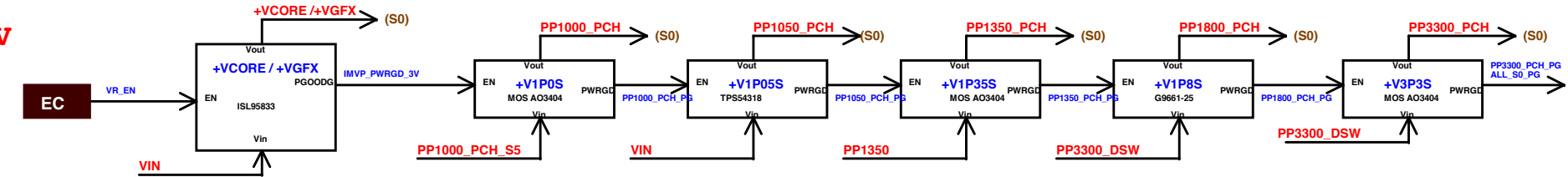
II



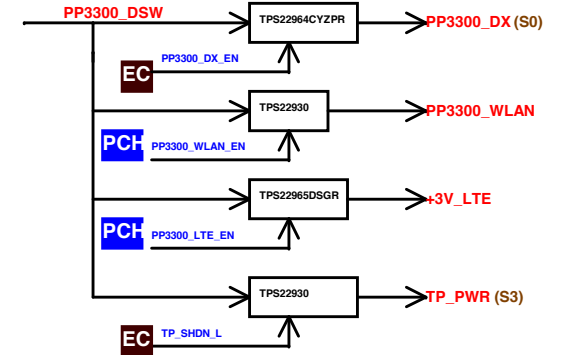
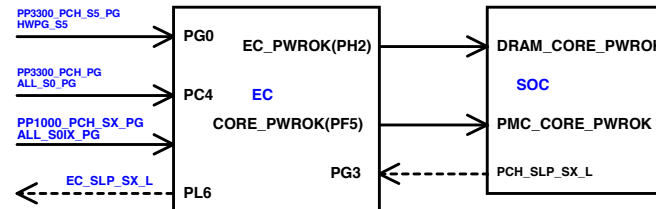
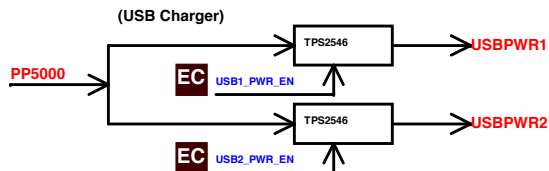
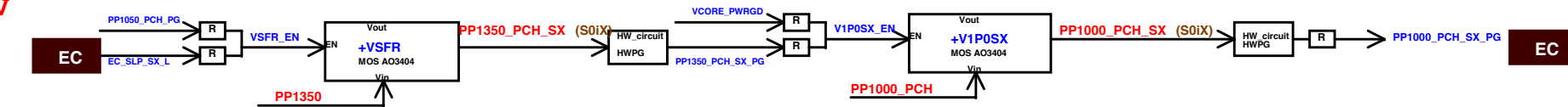
III





IV



V



		CHANGE LIST				41
Model	Version					
ZHS M/B	1A	1. 2015/05/19 :Update RAM ID for ZHQ and ZHS use.(page8) 2. 2015/05/19 : add R200 and R214 LTE_WAKE# and PMC_SUSCLK1 pull high to PP1800_PCH_S5 for can't into S3 issue (Page7) 3. 2015/05/19 : add R426 LTE_DISABLE# Pull-High to PP1800_PCH_S5 for can't into S3 issue.(Page 8) 4. 2015/05/19 : add R603/R609/Q62/R167/R607/Q63 FOR SD Card can't work issue. (page 17) 5. 2015/05/19 : add PR523 10k Pull-high to PP3300_DX for can't power on issue (Page 41) 6. 2015/05/19 : add PR234 and PQ35 for PP1050_PCH 放電線路 (Page 41) 7. 2015/05/19 : EMI request add PC189 for EMI issue. (Page 39) 8. 2015/05/19 : EMI request add C112 for EMI issue. (page22) 9. 2015/05/19 : EMI request add C130/C132 DMIC CLK/DAT for EMI issue(Page22)				
		1. 2015/06/19 : Add C35 and Change R326 to 33 ohm for Acer ESD request (page18) 2. 2015/06/19 : Add Pad1-Pad12 for Acer ESD request (page26) 3. 2015/06/19 : Add R427 33 ohm Acer ESD request (page27) 4. 2015/06/19 : Del R490 , Add R516 for SANYO battery 5. 2015/06/19 : Change 0 ohm to Short Pad: R14,R17,R39,R217 6. 2015/08/10 : Change 0 ohm to Short Pad: PR46,PR218,PR68,PR248,PR244,PR247,PR243,PR249,PR245,PR122,PR6,PR117,PR250,PR246				
DOC NO.	PROJECT MODEL:	Chrome	APPROVED BY:		DATE:	
	PART NUMBER:		DRAWING BY:		REVISION:	
		 Quanta Computer Inc. PROJECT : RAM Change list				

DOC NO.	PROJECT MODEL :	Chrome	APPROVED BY:	DATE:	 Quanta Computer Inc. PROJECT : EMS
	PART NUMBER:		DRAWING BY:	REVISION:	